Advanced Technology Development Program

Highly Integrated Electronics
Spacecraft Miniaturization
Spacecraft Communications
Advanced Architectures
Instrument-Enabling Technologies
Mission Autonomy
Model-Driven Implementation
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We are on the brink of the next era of space discovery. Technologies as broad ranging as new integrated digital/analog chips, miniaturization, communications, instrument technologies, autonomy, and modeling are key to future space missions. In the new millennium, we will need to achieve significant reductions in the size and power of system components and develop numerous new technologies to make concepts such as a micro-satellites and satellite constellations viable from a mass and power standpoint.

This Office of Space Science’s (OSS) Advanced Technology Development (ATD) program at The Johns Hopkins University Applied Physics Laboratory (APL) was a collaborative effort between APL, NASA’s Jet Propulsion Laboratory (JPL), and NASA’s Goddard Space Flight Center (GSFC). Our research efforts were linked to industry via specific technology subcontracts.

The primary objective of this $10 million, 2-year ATD program was to significantly improve the Technology Readiness Level (TRL) of critical spaceflight-enabling technologies. APL’s program was extensively targeted at TRL = 4–6, which corresponds to a technology readiness horizon of ~1–4 years. While the funding of specific projects was controlled by APL, the definition of the various projects was established in collaboration with APL, GSFC, and JPL teams, thereby ensuring appropriate focus and support of long-range NASA/OSS objectives.

Thirty-seven projects in seven technology thrust areas critical to ambitious, future space missions were targeted. These 37 projects, led by senior-level investigators, were focused on technologies that will enable evolutionary advances in a portfolio of technologies valuable in a wide range of prospective missions.

This publication provides summary final reports for these 37 projects, with introductions to each thrust area provided by the thrust area lead. The broad spectrum of technologies investigated culminated in significant advancements in understanding the processes involved in many spaceflight applications. In many cases, it culminated in brassboard development and demonstration of mission readiness at the Preliminary, and in some cases Critical, Design Review stage. Several projects, with significant industrial partnerships, were transferred to industry and are now available as line items in manufacturers’ catalogs. Others were of sufficient design and development maturity to be adopted into current NASA missions.

These projects can provide an impressive arsenal of tools for space-borne application and can significantly extend our capacity to conduct scientific endeavors and to understand more fully the nature of our planet, our solar system, and our universe.

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Highly Integrated Electronics

The Advanced Technology Development (ATD) program’s efforts in highly integrated electronics have focused on infrastructure requirements in spacecraft and instrument electronics. The goal of the work has been to reduce the resources (cost, mass, and power) necessary to implement circuit elements that are shared among multiple spacecraft and instruments.

Much of the cost of custom space-qualified electronics is not in the design stage but in the fabrication, packaging, testing, and qualification stages. The best way to lower the total cost of parts is to share them across multiple implementations by using parts that the user can configure (such as our field programmable arrays) or that are flexible enough to meet the needs of multiple applications. This is the driving motivator for electronics development at APL under the ATD program.

Schedule, cost, and performance can also potentially be improved through the use of commercial fabrication facilities and processes rather than dedicated radiation-hard facilities. Specialized design methods and tools have been developed in our ATD effort to implement radiation-hard designs using commercial foundry facilities.

Each of these methods has been embodied in our ATD highly integrated electronics developments, which are briefly described next. We have developed several promising technologies that can be used to dramatically lower the cost and risk of developing electronics for use in space. These technologies can also be used on Earth, and several are already being transferred to the commercial sector.

**Field Programmable Analog Array**

Almost all spacecraft and military systems contain numerous circuits that require moderate-performance analog and digital processing and input/output (I/O). These circuits are widely distributed throughout the system hardware and are used for applications such as status monitoring, motor and temperature control, and signal conditioning and processing.

Until now, these mixed-signal circuits have been almost exclusively implemented using discrete parts because the cost savings are not significant enough to justify a custom application-specific integrated circuit (ASIC) design. APL has designed a **field programmable analog array (FPAA)** under the ATD program that is compatible with Actel Corporation’s anti-fuse technology. This FPAA can be combined with existing digital programmable resources to create a chip that can be programmed to implement a general-purpose, programmable mixed-signal processing array. The advantages of using an FPAA are similar to those of using a digital field programmable gate array, namely, much lower parts acquisition and qualification costs, higher levels of integration, lower power, and faster turn-around design cycles. The FPAA would also improve overall reliability.

**Detector Processing Electronics**

Many “fields and particles” instruments share common signal processing needs. The electronics that implement these functions must often be very small to fit inside the sensor heads, and must run with very little power.

As part of our ATD effort, we have worked on a circuit known as an **Energy Chip**. It is
intended to contain the necessary electronics to detect and amplify small, fast current or voltage signals, shape and filter the resulting wave forms, and buffer the output for further processing. We have developed two versions of this chip. The first version contains a single processing chain plus a 10-bit analog-to-digital converter. This chip is intended to be mounted directly behind a detector, forming a full analysis channel. The second version of the chip contains eight parallel chains, where the peak signal outputs are internally sampled and made available for further off-chip processing. This is intended to support sensor designs that require simultaneous measurements from multiple detectors.

We have also developed a second generation of our time-to-digital converter (TDC) chip. This follows up on our groundbreaking ASIC, first flown on the IMAGE/HENA instrument, which can measure times in nanoseconds with a resolution of about 50 ps. Our second-generation device improves the performance of the earlier chip, fixes some known bugs, and extends the chip’s time range to support indefinite measurement periods.

**Microsatellite Support Electronics**

Several advanced ASICs have been developed under ATD to implement common spacecraft design or control elements. Of great interest has been the development of a microminiature digital solar attitude detector (DSAD), which can measure the Sun’s position to better than 0.1 degree resolution using only 25 mW of power and with a mass of 120 g and which transmits the digitized X/Y coordinates over a simple serial interface. This groundbreaking part can also be used as a moderate-resolution monochrome imager, thus acting as a “postage stamp” imager.

Several aspects of the Temperature Remote I/O (TRIO) chip that is being modified for the X2000 program were improved under the ATD program. Specifically, we researched improvements to implement an on-board radiation-hard voltage reference, expanded the address space, and qualified the part for operation under severe radiation environments at low voltages.

We have also developed a digital design library that enables a designer to use a standard Tanner Research Digital Design Library to implement a high-performance, radiation-hard circuit. This circuit design is then translated using a modified layout library to produce an ASIC design that can be fabricated in a standard commercial foundry to achieve high radiation tolerance and single-event-latchup immunity.
The arrival of digital field-programmable gate arrays (FPGAs) provided significant cost savings to the space electronics industry. These are chips that contain large arrays of simple, undedicated digital logic. End users, by means of software, can connect the simple logic modules together to make useful, powerful digital systems, with design cycles of days. By contrast, custom design of integrated circuits and board-level design using discrete components have design cycles of months; custom circuits can be prohibitively expensive for many projects, and discrete design increases system size, mass, and power consumption. The same considerations apply to analog and mixed-signal (analog plus digital) circuit design. Almost all spacecraft contain numerous moderate-performance analog and digital processing and I/O (input/output) circuits used for applications such as status monitoring, motor and temperature control, and signal conditioning and processing.

Field-programmable analog and mixed-signal arrays (FPAs and FPMAs) address this need for quick-turnaround time in analog flight hardware development. FPAs vary widely in the choice of the core programmable modules. The granularity of the module tends to be a function of the performance of the interconnect. Slower interconnect types, such as CMOS switches, have high resistance (≈1 kΩ) and are typically programmed with SRAM- and EEPROM-based memory. Such interconnects seriously degrade analog performance if inserted at arbitrary points in an analog design. Thus, modules for RAM-based analog arrays tend to have a large granularity, such as an entire filter section, and allow interconnect programmability only at certain critical points, such as between filter sections or in series with the resistor in the amplifier’s feedback loop. Faster (lower-resistance) interconnect types allow a finer module granularity, to the limit of gate array architectures, which allow programmability at the level of individual transistors but do not solve the problems of quick-turnaround time and flight qualification. Transitional “antifuse” interconnects offer a good trade-off between functionality and performance on one hand and quick development time and pre-flight qualification on the other.

The ATD program entered into a cooperative agreement with Actel Corporation, known for manufacturing radiation-tolerant and radiation-hardened FPGA parts based on its patented antifuse technology. We designed an FPAA test chip that was fabricated in a 0.25-μm, three-metal process, the same process used to manufacture one of Actel’s commercial radiation-tolerant product lines.

Circuit components are incorporated as resources that can be connected into the circuit individually using antifuses. In the original unprogrammed state, the resources are decoupled from the circuit except through the small antifuse capacitance. When programmed, the antifuses form connections between module resources with resistances of 209 Ω or lower. The low resistance of interconnects allows us to reduce the granularity of our core analog module to individual components comprising the following:

- 1 differential operational amplifier
- Programmable resistors (6 values in powers of 2, 2.5 kΩ to 80 kΩ)
- 8 programmable capacitor arrays (6-bit resolution, from approximately 0.5 pF to 31.5 pF)
- 32 complementary metal oxide semiconductor (MOS) (analog) switches
Our test chip incorporates 12 modules in a $3 \times 4$ array and can be used to implement many continuous-time and switched-capacitor circuits for standard spaceflight applications like pulse shaping chains, analog-to-digital and digital-to-analog conversion, modulators, oscillators, and filters.

Shift registers along the border of the test chip accept two bits that address an individual fuse by horizontal and vertical position, allowing external access to both sides of the selected antifuse for programming. There are over 30,000 programmable connections in the chip.

Actel’s RT-SX process meets the stringent requirements of radiation tolerance for spaceflight applications. However, it is a process refined for digital circuits and not well suited to traditional analog circuit design. This necessitates careful consideration of the analog module design and layout. Fortunately, this aspect of analog design has been a primary focus of research in recent years as a result of the wide availability of digital processes and the shrinking availability of dedicated analog processes. This research has produced, for instance, a wide variety of designs for CMOS operational amplifiers meeting our requirements for the FPAA. Our module amplifier is a two-stage differential design for a digital process (at 5 V) modified as necessary to maintain stability over the range of output loading capacitances possible by programming the module’s programmable capacitor array. We measured many standard characteristics of the amplifier. The amplifier shows excellent performance for a moderately simple two-stage design without offset correction.

Our goal for the ATD program was to demonstrate the feasibility of programmable analog components for the aerospace industry, attempting a short development by using an existing state-of-the-art digital fabrication process. With technical goals met, taking the project from research to commercialization ultimately rests with Actel and market forces. We have been actively seeking funding for a continuation of the project to improve the design and produce a commercial-grade part. One important consideration of a second-generation system would be the inclusion of digital circuitry to form a true mixed-signal array (FPMA).

The fabricated test chip, showing one of the 12 analog modules and examples of its major components.
Energy measurement is a basic function of many types of instruments (e.g., atomic particle, gamma-ray, and x-ray instruments). A single channel includes a low-noise preamplifier, a shaping amplifier, a peak detector, and a direct analog output or analog-to-digital converter (ADC). Several of these channels may be combined on a single chip to allow simultaneous processing of parallel signals. As part of this ATD effort, we have developed a circuit known as an “energy chip.” It is intended to contain the necessary electronics to detect and amplify small, fast current or voltage signals, shape and filter the resulting wave forms, and buffer the output for further processing.

The design challenges for complete energy chip channel implementations are low noise and high speed for a given power budget and detector size. Special attention is given to allocation of most of the power in the very front—in the preamplifier, where it is necessary to achieve low noise and just what is necessary in the follow-up stages for gain-bandwidth purposes. As soon as the optimum power distribution is achieved (with proper selection of circuit topologies), it is up to the user to select the power dissipation for a given noise figure and detector size. Another design challenge in this type of signal processing is to mix fast-switching digital functions with low-noise analog front ends. This was successfully addressed with the selection of current mode circuit topologies that minimize the digital noise as well as keep the analog function in low impedance.

We developed two versions of this chip: a single-channel energy chip and a multi-channel energy chip. The first version, developed as a custom application-specific integrated circuit (ASIC) fabricated by a foundry for radiation-hard silicon processes, contains a single processing chain plus a 10-bit ADC. This chip is intended to be mounted directly behind a detector, forming a full analysis channel. The second version of the chip, developed using a mask-programmable, radiation-tolerant mixed-signal array, contains eight parallel chains, where the peak signal outputs are internally sampled and made available for further off-chip processing. This chip is intended to support sensor designs that require simultaneous measurements from multiple detectors.

This project identified topologies for the chip designs and investigated the design of several types of front-end charge-sensitive amplifiers, including an external junction field effect transistor (JFET) option. Subsequently, we concentrated on the design of the low-noise preamplifier with an external JFET option for best detector matching and performance, a shaper/filter with optional settable gain and time constant, a peak detector, and a baseline restorer.

We also investigated the design of the ADC block element that could be used to process multiple channels of data. In addition, we investigated implementing digital control functions in the chip with analog (low-noise) circuits. Issues related to “classical” pulse signal processing versus fast sampling methods were considered, including sample-and-hold for an on-chip ADC with Wilkinson-type and flash-type ADC designs and research for peak detector circuit topologies.

The most critical parameter in the energy ASIC is the low-noise performance of the preamplifier. Test versions of the preamplifier and shaper stages were designed and modeled, including a few unique FET structures that might enable us to integrate the preamplifier input FET on chip.

Single-channel Energy Chip

As part of our custom ASIC approach, we have developed a complete energy measurement channel containing a charge-sensitive preamplifier, a semi-Gaussian filter, and an active baseline restorer. Charge-sensitive preamplifier variations were implemented to investigate optimum detector matching for noise and power dissipation. The semi-Gaussian filter was implemented for filtering and gain, and an active baseline restorer was developed to cancel offsets of the filter and remove pile-up effects.

Several test chips were fabricated:

- Energy 1. Includes a charge-sensitive amplifier (with an external JFET option), shaper-gain stage, and baseline restorer. This chip uses mostly internal components, with fine trimming via external components; it allows
characterization of high-level functions such as filtering.

- Energy 2. Includes a charge-sensitive amplifier (with an external JFET option), shaper-gain stage, and baseline restorer. This chip uses only external components for trimming; it allows independent characterization of each block of the channel down to the amplifier level.

- Alternate Amp. Includes an alternate core amplifier design for improved bandwidth and stability, and several block elements to test with reduced power supply (from 5 to 3.3 V and below).

Twelve Energy 1 and twelve Energy 2 chips were packaged in DIP 28-pin packages. Testing of the Energy 2 chip indicated that both versions of the charge-sensitive amplifier, the shaping amplifiers, and the baseline restorer are functional. Amplifier operation was tested using laboratory equipment to generate small tail-pulse signals. The baseline restorer operation was confirmed by measuring the transient response of the circuit. Preliminary test results verified the functionality of the various preamplifiers. DC functionality, stability, power dissipation, and noise with respect to detector capacitance were tested. In addition, the shaping time constant was tested for programmability in the range of 0.5 to 10 μs. Initial noise measurements indicated ~6 keV full width at half maximum noise at 10-mW power dissipation (~7 mW in the preamplifier), detector capacitance of 30 pf, 1.5-μs peaking time in the shaper, and baseline restore activated. The results indicate that ~20-keV particles can be clearly resolved.

Testing with the Energy 1 chip has been limited (due to the minimal component trimming we can implement), but it shows the expected functionality.

Our development schedule was critically affected by delay associated with the foundry for radiation-hard silicon. We spent many months investigating the functional and yield problems on several of those chips only to confirm that the foundry had internal process control problems that resulted in misalignments. No design problems were found to exist in the few devices we received that were functional. We have worked with the foundry to ensure that similar process problems will be avoided in the future. The full-up single-channel energy chip will be submitted for fabrication in mid-December and is not expected back for checkout until late spring of 2001. Further testing and qualification of the full-up design will be accomplished under the MESSENGER program when the devices return from the foundry.

**Multi-channel Energy Chip**

The development effort for the multiple channel device used a rapid prototyping and fabrication approach via a semi-custom configurable mixed signal array. This existing array is programmed by a custom metallization layer at the chip wafer level. The circuit design is based on one used for the Polar and IMAGE missions but has been heavily modified to provide much cleaner signal routing, additional capability, and a serial communications interface.

As seen in the accompanying figure, the resulting device contains eight separate energy channels, each of which has a charge-sensitive amplifier (with an external JFET option), shaper-gain stage, baseline restorer, fast and slow timing discriminators, and peak detector. Output signals are available separately or via a multiplexed output. The various circuit thresholds, enables, and operational modes are commanded over an internal I2C interface; this industry standard interface requires only two wires.

The full-up multi-channel energy chip design was submitted for programming in mid-December and is expected back in 6–8 weeks for testing. A big advantage of this design approach is that the cost and schedule for fabricating the device are far smaller than those required for custom ASIC designs. This allows any problems that are found to be rapidly corrected.
Time-of-flight (TOF) measurement is a basic function for many types of instruments (such as particle spectrometers, delay line imagers, and laser rangefinders) and can be a basic computational function for signal processing, e.g., analog-to-digital conversion. Generally a TOF system consists of the analog start and stop timing amplifiers, a fast comparator or a constant fraction discriminator (CFD), a time-to-digital converter (TDC), valid event logic, and read out.

A first TOF application-specific integrated circuit was designed at APL and was flown on the Imager for Magnetopause-to-Aurora Global Exploration (IMAGE) High Energy Neutral Atom (HENA) instrument. The HENA instrument determines the velocity, trajectory, energy, and mass of energetic neutral atoms (ENAs) in the energy range of 10–500 keV and from these data generates images of ENA source regions in the inner magnetosphere.

This TOF chip is essential to the accuracy of the HENA instrument since it determines the velocity of the ENAs that it detects by measuring their TOF and trajectory through the sensor, that is, from the entrance slit either to the back foil and two-dimensional imaging microchannel plate (MCP) detector or to the solid state detector (SSD). When an incoming ENA passes through the entrance foil, it produces secondary electrons, which are accelerated and steered to the front imaging MCP. This MCP (the “start” MCP) provides a start signal for the TOF analysis and registers the position at which the ENA penetrated the entrance slit. The ENA then continues through the sensor to the backplane and strikes either the foil in front of the two-dimensional imaging MCP or the SSD. In the first case, secondary electrons ejected from the back foil trigger a stop pulse in the two-dimensional imaging MCP, which also registers the position of the incident ENA. If the ENA strikes the SSD instead, the secondary electrons ejected by the impact are steered to the “coincidence” MCP, which provides the TOF stop signal; the position of impact is registered by the SSD.

The start and stop signals are processed by the analog TOF electronics in the HENA instrument’s main electronics unit. The start and stop pulses give the ENA’s TOF, while the position measurements reveal its trajectory and thus its path length within the sensor. With these two pieces of information, TOF and path length, HENA can calculate the ENA’s velocity.

Building on this past development, the ATD program developed an advanced TOF chip especially aimed at miniature particle instruments and laser rangefinding. Based on our test results, the radiation tolerance is sufficient to meet even the most demanding mission requirements. This ATD advanced TOF project included these activities:

- Programmable maximum time interval
- Improved dead time
- Improved/corrected valid events logic
- Recording on nonvalid conditions (double starts, stops, etc.)
- Improved/corrected operation at 3.3 V
• Improved phase lock loop (PLL) for better power supply, temperature, and radiation compensation
• Improvements in the CFD
• Reduction of cross talk
• Leading edge and constant fraction modes
• Optional pulse height analyzer in the CFD for time walk compensation as well as science extraction
• Study of integrated delay lines
• Study of general-purpose TOF-based signal processing
• Study of laser altimetry applications
• Study of telecommunication modulation/demodulation applications
• Fabrication and testing of prototype chips

The existing TDC design was first tested at reduced voltages (3.3 V) to determine which circuit elements needed improvement. The testing uncovered some weakness in the counter readout circuitry at these low levels. After discussions with the Jet Propulsion Laboratory to establish TDC requirements for communications (demodulation) applications, the ATD program evaluated the valid event control logic and PLL compensation circuit over a military specification temperature range and an increased total radiation dose. System-level considerations in terms of start-stop combinations and long-term stability were also studied.

We simulated the TDC core for operation at 3.3 V and compared the results with the measurement. A subcomponent test chip was completed and fabricated that contained optimized blocks based on the TDC-A characterization, including the basic timing and digitization cell, the PLL, the power supply, temperature compensation, and an I2C interface in the read-out. Also, the new TOF chip was designed in such a way that critical cells could be optimized without topology change. Optimization continued throughout the ATD program.

The ATD program also developed a post-processing software tool that locates errors in custom cells. It was successfully applied to the first-generation TOF design as part of the TDC upgrade process. Matlab was used for massive data processing and visualization of test results, which initially indicated that an organized substrate noise is coming from the PLL oscillator. We subsequently modified the design to minimize the substrate noise.

As a result of testing, the design layout was modified. The design and layout for the valid event logic block (rejection of double start, double stop, etc.) were finalized, and a new event accumulator was terminated in the existing block of three (to count starts, stops, valid events) and was finalized in the layout. The new accumulator counts nonvalid event conditions, so these elements provide complete information about the incoming event spectrum. A pulse height analyzer block was included for analyzing the start and stop signal strengths at 64 levels, which further corrected time walk produced timing errors and, most importantly, provided additional information for the spectrum of the incoming events. These measurements give a complete understanding of the incoming event spectrum.

Detailed simulations and worst-case analysis are continuing to verify all of the new design additions. The ATD program TOF chip will be used for a variety of future space missions.

http://sd-www.jhuapl.edu/ATD_NASAAPL/
Micro Digital Solar Attitude Detector

Many proposed missions depend on the use of “micro-satellite” constellations to make simultaneous measurements at different orbital locations. Numerous new technologies are required to make the micro-satellite concept viable from a mass and power standpoint. The apparent position of the Sun is an important spacecraft attitude measurement used by virtually all attitude determination and control subsystems. This measurement is commonly made with a sensor called a digital solar attitude detector (DSAD). A micro-DSAD (µDSAD) incorporating the entire sensor and its interface on a single chip would enable one to create a sensor small enough to be used in micro-satellites for spacecraft formation flying and applicable for nearly all NASA spacecraft missions. The position-sensitive detector should ideally be integrated on the same chip as the support electronics. Because this is difficult and costly to achieve with a charge coupled device (CCD) detector, a detector compatible with complementary metal-oxide semiconductor (CMOS) processing is desirable.

As part of the highly integrated electronics thrust area of the NASA Advanced Technology Development program, APL has developed the first generation of such a µDSAD integrated circuit for use in micro-satellites. The µDSAD design is based on our patented approach of combining a centroiding position-sensitive active pixel architecture with standard imaging capability for providing optional housekeeping images. The X and Y coordinates of the light-intensity centroid are calculated on chip and can be directly read out of the chip over the simple serial interface. This approach avoids the need for a digital signal processor to compute the position, thus dramatically lowering the required mass and power resources. In addition, the design approach does not require any of the high-voltage, high-transient current peripheral clocking circuitry needed by most CCD detectors.

The µDSAD is a multi-faceted instrument that meets the requirements for the Sun sensor needed as part of ultra-low-power electronics and avionics and that can also be used as a medium-resolution imager for monitoring solar panel, boom, and antenna deployments or for sighting stars or other items of interest. Readout rates in either the Sun sensor or imager mode are limited primarily by image integration times and the serial output bus speeds. Approximately 5000 solar position readouts or image pixels can be read out of the sensor per second. The complete sensor should require less than 50 mW and weigh about 120 g.

The µDSAD technology has been brought up to technical readiness level (TRL) 4. We have...
designed, fabricated, and tested a 64 × 64 pixel version of the µDSAD application-specific integrated circuit (ASIC) design. Our layout style enables us to use commercial CMOS foundries and avoid the costly use of dedicated radiation-hardened processes. We have selected the AMI C5N process (0.5-µm process) for our designs because AMI is committed to maintaining it (longevity) and it is available for low-cost prototyping through the MOSIS service.

We performed radiation testing on the prototype µDSAD chip. The apparent gain change after radiation was negligible, but we cannot measure absolute offset shifts with our current equipment. It is clear, however, that the basic position-sensitive active-pixel method is quite radiation tolerant and is sufficiently accurate for a wide range of applications. A second DSAD2 chip was dosed to high kilorad levels and exhibited no apparent performance degradation. These test data show that the annular NMOS layout technique provides excellent total dose immunity with the AMI C5N process. The DSAD2B prototype chip was tested for single event latchup (SEL) at Brookhaven National Laboratory and found to be SEL immune for a linear energy transfer (LET) of 120 MeV·cm²/mg. Using this prototype design, we have demonstrated robust performance, high total dose radiation tolerance, and SEL immunity.

A full-featured 200 × 200 pixel µDSAD (DSAD3) has been fabricated with the same C5N process and is available for checkout. This chip requires only an external field-programmable gate array, a bypass capacitor, and appropriate optics to function as a DSAD sensor. It provides an I2C interface (four wires, including power and ground) and is predicted to dissipate less than 20 mW. The 200 × 200 µDSAD includes several analog support circuits, including a 10-bit, successive-approximation analog-to-digital converter, an analog multiplexer, a bias generation circuitry, a readout amplifier, a clock generator for the digital support circuitry, and a voltage reference. An SRAM (static random access memory) chip will also be put on the test board to facilitate simple readout for the imager mode.

Using a simple single element lens, the 64 × 64 pixel device was able to determine the Sun’s position with 0.5º resolution over a 30º field of view (FOV); the larger 200 × 200 array should improve both the resolution and FOV. We also took a sample picture with this device to demonstrate its ability to acquire useful images.

Additional work remains to bring this device from TRL level 4 to a flight-qualified design. By increasing the size of the array to 512 × 512 pixels, we hope to achieve better than 0.1º resolution over a 100º FOV. The smaller arrays can view the same FOV with reduced resolution.

Possible uses for the imager include viewing of star fields, celestial objects, and deployable structures.

http://sd-www.jhuapl.edu/ATD_NASAAPL/
Radiation-Hard Digital Design Library

We have also developed a digital design library that enables a designer to use a standard Tanner Research Digital Design Library to implement a high-performance circuit. That circuit design is then automatically translated using a modified layout library (which we have licensed to Tanner Research) to produce an ASIC design that can be fabricated in a standard commercial foundry to achieve high radiation tolerance and SEL immunity. Test chips that we have created using this design flow and that have been fabricated commercially at AMI have been successfully tested at APL to 300 krad and have proved to be SEL immune when tested at Brookhaven National Laboratory. The design library will soon be available to the entire space community.

Digital Isolator ASIC

We have worked with the The Johns Hopkins University to develop a “transformer isolated” digital buffer ASIC. This device is intended to replace radiation-sensitive opto-isolators for space applications. Since our work on this project has started, the Analog Devices Corp. has produced a similar design (designated the ADum1100). Both devices use on-chip oscillators to amplitude modulate a signal across an on-chip inductive transformer, then demodulate it on the other side. For our design, we use an oscillator frequency of approximately 900 MHz.

Our device, designed at The Johns Hopkins University, is expected to be extremely radiation-hard as a result of the fabrication rules and the process we are using. It is designed to handle data rates >50 MHz and will require <15 mW per isolator, compared with 50 mW for slower opto-isolator devices. We are designing for primary to secondary voltage breakdown of 100 V, but have a goal of 1000 V. Because the device will not suffer optical degradation, which commonly occurs in opto-isolators under radiation, it will be useful for ground isolation, bus fault isolators, power converter isolation, etc.
The remote input/output (RIO) smart sensor chip is APL’s mixed analog-digital, radiation-hardened, low-power, data acquisition device suitable for spacecraft and instrument data collection. The chip communicates over a standard serial I²C bus or a standard parallel bus. RIO, in its complete version, will measure temperatures using external thermistors, total ionizing dose using external rad field-effect transistors (radFETs), voltages, and currents. Its sensing capability can extend to other physical quantities such as photons and vibration. A first version of this chip is focusing on temperature measurements only (TRIO chip). TRIO measures 16 temperature channels using external platinum resistance thermometers. It can also measure voltages only, using an external voltage reference. The TRIO chip contains comprehensive front-end analog conditioning circuitry, the analog multiplexer, a 10-bit analog-digital converter (ADC), memory, and both a serial I²C and standard parallel interface. TRIO can operate in a fixed mode, where only a particular sensor is addressed then digitized and read out, or in a scanning mode, where all 16 sensors are sequentially and continuously scanned, digitized, stored into self-contained memory, and then read out. This single chip system will be a valuable enabling technology for next-generation small spacecraft.

This ATD program started detailed electrical testing of existing first-generation TRIO chips at 3.3 V ±10% operating voltage and in the required temperature range (−55°C to +125°C). Under this ATD project, building blocks (such as the front end, the ADC, the memory, and the I²C) as well as the complete chip were evaluated and characterized, and design modifications were applied. This portion of the ATD program was a major technological advancement since the new operational standards consistent with the NASA X2000 spacecraft were introduced.

During the ATD program we also conducted detailed radiation testing up to 4 Mrad total dose at the 3.3-V operating voltage. The radiation testing to such a high total dose was a major achievement made more difficult by the 3.3-V operation because of, e.g., threshold shifts. Building blocks (such as the front end, the ADC, the memory, and the I²C) as well as the complete chip were evaluated and characterized, and design modifications were applied. This work was a major technological development advancement given that the chip is a mixed analog–digital device and the operating voltage is 3.3 V.

This project also started chip development of an on-chip voltage reference for 3.3-V operation. The voltage reference is a critical function of the ADC in the voltage mode of operation. This design effort used test data generated under this program.
Spacecraft Miniaturization

Ark Lew

Electronics miniaturization of space hardware is an enabler of innovative, low-cost missions for Government programs and commercial space ventures. Small electronics form the basis for micro-instruments/payloads and micro-satellites that enable missions involving single or multiple satellites. Micro-satellite based formation-flying missions can implement innovative sensing technologies that are impractical with conventional approaches. Multiple satellites flying in loose formation permit remote and \textit{in situ} sensing of physical phenomena that provide data for three-dimensional analysis to yield additional insights, whereas multiple satellites flying in tight formation enable space interferometric science. With the development of micro-satellites, instant constellations can be facilitated in one single launch using smaller, low-cost vehicles to support defense and industrial initiatives. Furthermore, miniaturized spacecraft infrastructure allows additional miniaturized payloads to provide more scientific data for commercial ventures and for the DoD. The spacecraft miniaturization initiative of the ATD program has achieved significant reduction in size, weight, and volume for implementing miniaturized, space-based electronics systems. This ATD thrust area has also studied new processes that enable sensors to operate at cryogenic temperatures; the design of an integrated power source (IPS) that is the basis for highly autonomous power generation and distribution; the design of small, reliable high-voltage power supplies; and the packaging of miniaturized, commercial off-the-shelf (COTS) equipment for space applications.

One of the tasks for the spacecraft miniaturization ATD thrust has focused on flip-chip bonding of large, cadmium zinc telluride (CdZnTe) arrays (4096 flip-chip bump contacts) to silicon application-specific integrated circuit (ASIC) processor chips. Indium is desirable as an interconnect metallurgy because of its excellent fatigue characteristics at cryogenic temperatures. The bonding of these large detector dies (approximately 28 mm$^2$) was not successful previously, primarily because of the inadequate height of the indium bumps (10–15 $\mu$m). Small amounts of camber in either the CdZnTe array detector or the silicon processor chip can cause the bumps on either device to pull away after bonding, resulting in open circuits. To improve the flip-chip bonding yield, the height of the indium bumps must be significantly increased. In this ATD task, several novel approaches for fabricating tall indium bumps have been investigated.

The application of flip-chip interconnections in electronic packaging can achieve smaller size, better performance, higher reliability, and, with the development of new materials and processes, lower cost. Under the same ATD thrust, we have investigated the feasibility and reliability of several types of interconnect technologies for flip-chip packaging to support future space applications. We have focused on the reliability study of interconnections between integrated circuits (ICs) and the substrate, as they appear to be weak linkages for long-term reliability. Emerging interconnect technologies, including anisotropic conductive adhesive with Au/Ni bumped dies, nonconductive paste with Au stud bumped dies, and isotropic conductive paste with Au stud bumped dies, as well as conventional solder processes have been investigated in this ATD task.

Substrate design plays an important role in the miniaturization of electronics. The rapid development of ultra-high-density ICs can only be implemented with advances in compatible and reliable high-density interconnect printed wiring board technologies.
Micro-vias, including blind and buried vias, can effectively permit signal routing of high input/output density ICs. Micro-via technology demonstrates further advantages when implemented with area array ICs, such as flip chips and micro ball grid arrays, that typically require a tremendous number of signal lines in very small areas. The use of micro-via technology in space electronics can lead to significant reduction in size and weight for future space missions. In this study, we have investigated several methods of developing reliable, low-cost, high-density substrates with micro-via technologies.

Existing spaceborne Global Positioning System (GPS) receivers and navigation systems are much larger and more expensive than modern spacecraft designers can tolerate. With the evolving trend toward low-cost satellites and missions and toward formation flying with distributed spacecraft mission architectures, lower cost, more highly integrated, and lower power GPS navigation systems are needed. Radiation tolerance and system-level autonomy are also critical requirements for future systems. The ATD program has developed in part space-qualified, miniaturized, highly integrated GPS navigation and crosslink communications systems as a critical enabling technology for a host of individual and distributed spacecraft Earth science missions.

The implementation of miniaturized electronic hardware requires adopting innovative high-density electronic packaging designs. Although chip-on-board (COB) technology and three-dimensional die stacking are now used in consumer and computer electronics, reliability is not a critical issue for these commercial applications. The goal of this ATD program is to demonstrate space applicability of the APL COB process, through fabricating and testing a processor module with complete functionality and complex application. The module is designed to communicate with similar modules using the IEEE-1394 serial bus, using modular, stackable schemes. The board design includes bare dies, Actel field-programmable gate array (FPGA) die packaged on snapstrate adapters, a laser programmed ASIC die, packaged semiconductors, an infrared transceiver, miniature nanonics input/output connectors, and a fuzz button inter-board connector.

Prior miniaturization efforts have encountered problems while developing high-voltage power supplies for onboard science instruments. Scaling down the size of high-voltage circuits is fraught with breakdown and coronal discharge problems that can seriously damage the instrument electronics. The primary objective of this ATD study is to develop advanced techniques necessary to design miniature high-voltage circuits that can be qualified for safe and reliable space flight operations. We investigated the behavior of high-voltage circuit designs with respect to changes in dielectric and conductive materials, conductor lengths and shapes, and topologies of ground planes. The selected techniques and designs are demonstrated in the miniaturization of a five-stage Cockroft-Walton circuit that generates 5 kV.

The Integrated Power System (IPS) is an enabling technology for new microsat architectures in which dedicated power sources provide regulated power for spacecraft instruments and subsystems. The IPS is a thin, independent panel that comprises an integrated assembly, including solar cell array, housing, battery, and charge management system, rather than a set of separate components and, therefore, offers improved packaging efficiency. The energy storage layer is implemented as a matrix of batteries. Different battery chemistries, including lithium ion, lithium ion polymer, and solid-state polymer, can be accommodated by firmware. The microprocessor-based power management electronics autonomously control the charging and discharging of the embedded batteries to provide energy storage, distribution, accurate coulometry, diagnostic monitoring, and graceful degradation in the event of a battery failure.

Various methods for digital information storage and retrieval exist for spacecraft applications. Solid-state recorder boards (memory chips) and tape devices have provided this function in the past at the expense of high cost and large volume and mass. This ATD task has concentrated on packaging a set of commercial disk drives for a spacecraft environment to leverage on available commercial technology without the need for custom-designed, mission-specific storage devices. Laptop disk drive technology has approached the level of ruggedness required for spacecraft flight in a number of areas. The major effort has been to develop a flight enclosure to adequately package the drives (vacuum seal, thermal, material selection, mass, volume, electrical and mechanical spacecraft interfaces, radiation shielding, etc.).
Indium Bumping and Flip-Chip Technology for Cadmium Zinc Telluride Detector Arrays

NASA has expressed strong interest in flip-chip bonding large, cadmium zinc telluride (CdZnTe) 64 × 64 arrays (4096 flip-chip bump contacts) to application-specific integrated circuit (ASIC) processor chips for use in infrared detector focal planes in hard x-ray astrophysics applications. Indium is desirable as an electrical interconnect material for this application since it has excellent fatigue characteristics at cryogenic temperatures. To date, these large detectors (approximately 28 × 28 mm) have not been successfully bonded primarily because of the small height of the as-fabricated indium bumps (10–15 μm). Small amounts of camber in either the CdZnTe array detector or in the silicon processor chip can cause the bumps on both devices to pull away after bonding, resulting in open circuits. To improve the flip-chip bonding yield, the height of the indium bumps needs to be significantly increased. The small size of the contact pads (15 μm wide × 30 μm long) makes fabricating tall bumps (>20 μm) extremely challenging.

This ATD project enables us to develop an indium bump bonding process for fabricating fine-pitch, large-area detector arrays for gamma-ray and cosmic-ray imaging detectors. APL used its new high-pressure flip-chip bonder to develop a low-temperature bonding process to attach a CdZnTe detector to the ASIC processor. An underfill epoxy material was applied to fill the gap between the bonded chips for improved reliability and increased strength of the interconnects. The complete bonding and epoxy underfilling process had to be done at or below 80°C since CdZnTe detectors have been known to degrade when exposed to temperatures above 100°C. Since indium melts at about 150°C and epoxies typically cure at temperature above 125°C, this project necessarily involved overcoming some significant manufacturing challenges.

We bonded this “new” simulator ASIC to a simulator detector chip using the “pre-bond underfill” process and obtained electrical continuity on 62 of the 64 columns on this chip assembly. The total daisy-chain resistance varied from 600 to 1600 Ω from one end of the column to the common ground connection. (The sheet resistance of the aluminum traces caused...
much of the resistance.) All of the electrically fixed columns, as well as most of the other columns, exhibited continuity. The bonding force must have penetrated the thin oxide layer during the bonding process to cause so many of the other columns to conduct.

In the pre-bond underfill process, the adhesive was first applied to the surface of the detector chip and the chips were then aligned and bonded together without heating. Pressure was maintained while the heater was activated on the flip-chip bonder to cure the adhesive. The adhesive was squeezed out from between the indium bumps during bonding as a result of constant applied pressure without interfering with the electrical contact. Although this process is still being developed and will need to be further evaluated to prove repeatability and reliability, we have demonstrated a 96.8% yield for electrical conductivity on a large-area array.

Advanced Interconnect with Flip-Chip Technologies

Flip-chip interconnect technology has grown extensively with the demands for high-density packaging and electronics miniaturization. The use of flip-chip interconnections can potentially achieve smaller size, better performance, higher reliability, and, with the development of new materials and processes, lower cost. We investigated the feasibility and reliability of several types of interconnect technologies for flip-chip packaging to support future space applications. We focused on the interconnections between integrated circuits (ICs) and the substrate since those interconnections appear to be weak linkages for long-term reliability. This study investigated emerging interconnect technologies, isotropic conductive paste (ICP), nonconductive paste (NCP) with Au stud bumps, anisotropic conductive adhesive (ACA) with Au/Ni bumped dies, NCP with Au stud bumped dies, as well as conventional solder process.

Flip-chip interconnect technology supports high-density interconnect without compromising component size and weight since it uses the entire area underneath the die rather than just the peripheral area of the die. Flip chips provide better thermal performance and faster signal speed compared with packaged ICs because an entire level of packaging is eliminated. Advantages of the advanced flip-chip alternative interconnect technologies are as follows:

- Potentially smaller, thinner, and lighter products. Solder bridging and brittle intermetallic formation can be avoided to permit higher input/output density.
- Applicable for flexible substrate and temperature-sensitive component. Some of the interconnect materials can be cured at lower temperature than solder, or even with ultraviolet light.
- Similar to conventional solder interconnects in process procedures. Some combinations of the die bump metallurgy and interconnect materials can achieve both electrical interconnection and mechanical strain relief in a single process, eliminating the entire step of underfilling. The simplified process can lead to cost saving and shorter assembly time.
- Feasible for small quantities of product, such as spacecraft electronics. Unlike the conventional solder bumping process that requires the entire wafer, Au stud bumps can be performed on individual dies. This could result in significant cost saving, especially when minimum quantities are required.
- Potentially better performance in areas of electrical, structural, and thermal behaviors.
- Environmentally benign without lead contamination from the traditional solder material.

The advantages of adhesive flip-chip interconnect technology are so inviting that industries, especially those of handheld electronics such as cellular phones and camcorders, have incorporated such technologies into their commercial products. Unlike solder interconnect, whose physical, mechanical, electrical, and thermal behaviors have been thoroughly studied, whose long-term reliability has been carefully examined, and whose failure mechanisms are sufficiently understood, the long-term reliability of adhesive flip-chip interconnect technology, especially in severe environments such as the outer space beyond the Earth’s atmosphere, is still being investigated.

The objective of this study was to investigate the feasibility and reliability of using the advanced flip-chip interconnect technologies, as well as the traditional flip-chip solder interconnects, for space application. Au stud bumped dies (with or without coining), Au/Ni plated dies, and solder bumped dies were chosen to be the die metallurgy for this study. Interconnect materials used in this study included ACAs, ICPs, NCPs, solder, and underfill materials. A matrix of interconnect technologies investigated in this study is shown in Table 1. Selection of these technologies is based on new studies in which such combinations of die metallurgy and interconnect material demonstrated promising results in reliability.
Advanced Electronic Packaging

Wire bond is then attached to the substrate by conductive epoxy. Flip-chip technology using wire bonding for making electrical conductive on the die and the traces on the printed wiring board (PWB). With applied pressure and elevated temperature, an electrical conductive material is trapped in between the bond pads. The tails of the wires are then removed, leaving the studs on the die surface for the next assembly. This technology can be used on individual dies instead of on the entire wafer, which could result in significant cost saving when only several dies are needed. During assembly, under pressure and heat, the Au stud bumps penetrate the NCP material and form electrical connectivity through metal-to-metal contact. At the same time, the cured NCP acts as mechanical bonding and strain relief, eliminating the need for additional underfill material.

ICPs are being tested for flip-chip interconnects and have demonstrated promising results. ICP is an electrical conductive material that is applied on top of flattened Au studs prior to assembly. The electrical interconnection between the Au bumps on the die and the conductance on the board is achieved through the ICP material, which also provides mechanical and thermal connection.

We have worked with the University of Maryland Computer-Aided Life Cycle Engineering Department (CALCE) to evaluate the fundamental physics of failures and to select potential material candidates for the interconnects and the underfill epoxies. During the material evaluation process, we used glass substrates to evaluate the bonding processes with respect to temperature, pressure, and time. CALCE performed micro-sectioning to evaluate conductive path formation in the depth of the adhesive material using an environmental scanning electron microscope. We have also worked with Toshiba to get their latest ACA and NCP products. We subcontracted with Fraunhofer Institute Reliability and Microintegration to use their test dies, facilities, and expertise for flip-chip assembly using various interconnect materials that APL provided. We leveraged on the flip-chip technologies developed by HyComp (located in Marlborough, MA) for DARPA programs. HyComp is among very few domestic companies that can perform some flip-chip assembly work using conductive and nonconductive adhesives for small quantities.

We have developed a process for gold stud bumping on individual dies. Automatic ball bonding equipment was used to achieve better parameter control and speed. Parametric studies of various bonding energy levels and ball sizes were conducted, followed by ball shear tests, in order to determine optimum stud bumps. The results of our gold stud bumps profile and shear test results were compared with dies gold stud bumped by Fraunhofer. We performed the same assembly tasks with NCP using APL gold stud bumped dies to further confirm the quality of our gold stud bumps, and we have successful results from the APL-developed Au stud bumping process. We can

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<th>Table 1. Matrix of interconnect technologies investigated.</th>
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<td>Au stud bumped die (with coining)</td>
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<td>Au stud bumped die (without coining)</td>
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<td>Au/Ni plated die</td>
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<td>Solder bumped die</td>
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Anisotropic adhesive flip-chip technology. Stud bumps (single-ended wire bonds) are used with anisotropic adhesive layers. (a) Particle details. (b) Double-layer anisotropic conductive adhesives or films exist; only put conductive particles in the vicinity of the bump–board metallization interface (saves cost).

Flip-chip technology using wire bonding for making a gold bump on standard chip metallurgy. The chip is then attached to the substrate by conductive epoxy followed by an underfill as necessary.
achieve not only a comparable profile of the Au studs but also similar shear strength compared to the Fraunhofer process. We have also assembled Ni/Au plated dies on polyimide PWBs using two different types of anisotropic conductive pastes (ACPs) with promising results.

We completed the fabrication of a test board design that included test structures for the four-point resistance measurements and two-point daisy-chained resistance measurements to study the in-situ behavior of the flip-chip technologies during the environmental tests. The 1000-temperature cycle test is still under way, with promising early results with the NCP and Au stud bump technology.

**Ultra-High-Density Substrate Design with Micro-Via Technology**

This advanced packaging project has investigated methods of developing and conducting reliability assessment of micro-vias in low-cost, high-density PWBs and methods of implementing high-density PWB design in board layout to reduce system weight and volume. Typical micro-via hole diameters range from 0.05 to 0.25 mm. These vias are divided into three categories: blind, buried, and through-hole. Blind vias provide the interconnection from the outer layer to an internal layer. Buried vias provide interconnection among internal layers. Both of these features reduce the occupied surface areas, which can lead to significant reduction in space electronic system size and weight. In the conventional PWB, a mechanical drilling process is used when the via size is greater than 0.25 mm. For smaller holes, laser-drilling processes are required.

We evaluated two laser-drilling processes: conformal-mask drilling and full-via formation. For conformal-mask drilling, the outer copper is chemically pre-etched by a photolithographic process to expose the dielectric layer. A CO$_2$ laser beam is then focused onto the surface of the PWB to ablate the dielectric material and form the hole. After drilling, the PWB is cleaned by plasma etching prior to the electroless copper plating step to ensure a clean surface for subsequent plating steps. The full-via formation drilling process with dual lasers uses an ultraviolet (UV) laser in combination with a CO$_2$ laser. The UV laser is used for ablating the copper layer, and the CO$_2$ laser is used subsequently to ablate the dielectric material in the via formation. This process also requires cleaning after drilling prior to the electroless copper plating. The potential advantage of the full-via formation is the elimination of the tedious inspection step that is required in the conformal-mask drilling to ensure that all copper areas are etched properly before the laser drilling step starts. For the buried vias, we tested two types of via formations: filled and unfilled vias. The filled via configuration used conductive epoxy that is forced into the vias before the final lamination of all PWB layers. This process eliminates the potential of having voids in the vias, which could become a reliability concern when inadequate prepreg material failed to fill up the vias during lamination.

A very critical step in micro-via fabrication is the deposition of electroless copper after the holes are formed and cleaned with glass etching, plasma etching, etc. We evaluated two plating processes: the conventional direct-current plating process and the pulse plating process. In the pulse plating process, the supplied electrical input is turned on and off repeatedly with adjustable duty cycle and frequency. The agitated/regulated current induces more even ion distribution, which leads to better copper ion deposition and plating quality for blind holes with high aspect ratios.

To support this study, we worked with HADCO, a MIL-certified PWB manufacturer located in New Hampshire. Both HADCO and APL built test boards with micro-via structures to evaluate the performance of such a design using two completely different manufacturing processes. The design included daisy-chained patterns and was subjected to a 1000-thermal-cycle test from −55°C to 125°C. We also performed microsection inspection of the test coupons and the PWBs to obtain the correlation between the as-built and post-test conditions. The results from this project complement the existing military specifications, which do not provide a guideline for micro-vias. Our test results indicated that micro-vias larger than 0.15 mm are reliable and can support future space missions.
The use of autonomous Global Positioning System (GPS) navigation systems on Earth science missions will result in lower-cost programs by greatly increasing the level of spacecraft autonomy, thereby reducing mission operations costs. It has also been demonstrated that the use of spaceborne GPS increases the scientific return of Earth science missions by providing on-orbit real-time and ground-based orbit determination. Furthermore, designs have been developed at APL, funded by NASA Goddard Space Flight Center, for integrated GPS positioning, cross-link communications, and relative navigation systems. With the TIMED mission design, GPS systems have been shown to be critical for event-based commanding mission operations. With the decision by the GPS Joint Program Office to embark on a modernization program that will provide two additional civilian frequencies, it is clear that the importance of spaceborne GPS applications will continue to grow.

A miniature GPS Navigation System (GNS) receiver card, compatible with APL’s 100 × 100 mm Command and Data Handling in Your Palm (C&DH-IYP) system, was based on the flight-qualified TIMED GNS system but includes a number of improvements and enhancements. Part of this effort included support of embedded passive component technology research. The card functions as the master in a master/slave configuration where a slave card supports the second and third GPS civilian frequencies and a cross-link transceiver used for formation-flying communications and relative navigation. The card incorporated the TIMED GNS’s Tracking ASIC (application-specific integrated circuit) (GTA), a 200,000-gate, >1-Mrad (Si) gate array that includes 12 GPS tracking channels, timing and control circuits, and a processor interface.

The packaging design for the ATD GNS receiver module is based on a three-dimensional interconnect technique by which electrical connections between modules were made via a fuzz button connector in lieu of a motherboard. Each module is mounted on an aluminum frame with direct access to the base plate for thermal control. This approach provides flexibility to accommodate future expansion and modification of the design by simply adding or replacing one of its modules. The circuit board design in this project is three times smaller than the one used in the TIMED spacecraft. We achieved this size and weight reduction by eliminating the center core heat sink and the individual compartments in the previous design. In this design, we demonstrated that the thermal control of the board can be achieved with the internal power and ground planes in the board design. We also demonstrated that, by using proper ground plane layout, cross-talk between subsystems can be eliminated. The thermal analysis of the GNS receiver module indicated that all component junction temperatures are within the design limits.

The printed wiring board design for the GNS receiver module has two signal layers, one power layer, and three ground layers. It is 100 mm long and 100 mm wide and approximately 1.6 mm thick. Both power and ground layers use 1 oz.
(28 g) of copper plane, which is equivalent to 1.4 mil of copper in thickness. All signal layers use 1 oz of copper material and have a routing density of about 10% of the available surfaces. The top and bottom layers use 1 oz of copper material and have a routing density of about 20% of the available surfaces. The board material is polyimide glass to minimize excessive thermal stress in the plated through holes during the high-temperature soldering process. Active and passive components are mounted on both sides of the printed wiring board, further enhancing the packaging density.

We used the COSMOS finite element program for thermal analysis of the GNS receiver module. The COSMOS math model contains 608 thin-shell, 4-node elements. The printed wiring board is modeled as one single layer of copper to represent four layers of 1-oz copper planes. Power dissipations of active parts are applied as nodal powers at approximate node locations. The aluminum frame and the board stiffener are also modeled. Because the printed wiring board is attached with the frame through fasteners at seven locations, not all nodes at the board/frame interface are merged together. The discontinuity of the temperature distribution among certain areas of the board/frame interface reflects this boundary condition. The mounting feet of the frame were subjected to a uniform temperature of 60°C. This base plate temperature was derived from previous satellite designs at APL. The results from the board finite element analysis were used in the final calculation of the device’s junction temperatures. The junction temperature calculation is based on the board temperatures and the device junction-to-board thermal resistances. If the information was not available from the manufacturer, conservative assumptions were made in the thermal resistance calculations.

A design was also developed and prototyped for an advanced version of the TIMED GTA gate array, called the GTA-Follow On (GTA-FO). The GTA-FO incorporated advances to enable GPSs based on this device to satisfy a number of different mission requirements, including sole-means attitude determination, cross-link communications and relative navigation, and remote sensing. The resultant systems dissipate less power, recover data using the additional GPS modernization signals, and have improved autonomous operations. The GTA-FO design incorporates an integrated 32-bit integer processor, greatly increasing the level of integration and reducing the eventual power dissipation. This ATD initiative developed the detailed GTA-FO architecture and developed a simulation written in the C language. The simulation of the GTA-FO tracking channel was used to track simulated GPS signals to prove viability of the design.
The shift in emphasis to smaller, better, and cheaper spacecraft, resulting from the NASA New Millennium Program and similar initiatives in DoD-sponsored programs, demands highly innovative designs that traditional electronic packaging cannot meet. Conventional electronic packaging uses surface-mounted or through-hole components. These approaches require significant board surface area and associated mass in order to accommodate the electronic component body and leads. Chip-on-board (COB) technology, where active die are directly mounted onto a substrate without the need for an intermediate package, provides a process to significantly miniaturize electronic hardware.

APL has developed a unique COB process for high-reliability spaceflight hardware applications. The APL COB process supports both bare die and packaged parts and accommodates rework, unlike some of the other miniaturization technologies. Using COB technology, a standard design for miniaturized, stackable electronic modules has been developed under the ATD program’s Command and Data Handling in Your Palm (C&DH IYP) project.

In order to maintain structural integrity while minimizing size and weight, the C&DH IYP system needed to be carefully designed to withstand the harsh vibration environment encountered during satellite launch and to maintain acceptable thermal limits that would be encountered over a wide range of missions. Finite element models were generated and vibration and heat transfer analyses were conducted to verify the thermal and mechanical design.

The module chosen for implementation in the ATD program was the RTX2010 Processor and Interface unit that was developed into a proven breadboard evaluation unit under a previous NASA Goddard Space Flight Center C&DH IYP grant. The module consists of a $10.2 \times 10.2$ cm magnesium frame that encloses and supports a 10-layer polyimide multi-layer printed wiring board. The module is designed to stack with other modules using a “fuzz button” stackable connector. The stackable connector implements a virtual backplane that carries power, ground, and signals to each module in the stack. Communications between stacked modules is implemented with a redundant IEEE-1394 serial bus that runs through the virtual backplane. The selected board design is an excellent vehicle for demonstrating the APL COB process because it includes devices with a variety of package types. The board design includes bare die, Actel field-programmable gate array (FPGA) die packaged on snapstrate adapters, a laser-programmed application-specific integrated circuit (ASIC) die, packaged semiconductors, an infrared transceiver, miniature nanonics input/output connectors, and a fuzz button interboard connector. As a further challenge for the COB process, the laser-programmed ASIC has a dual ring of bond pads that required the pads on the board to be staggered on two different board layers.

The RTX2010 module implemented with the COB process has a mass of 105 g and dissipates 3.2 W with the processor running at full speed. The substrate used in the C&DH IYP module was fabricated in APL’s polyimide board fabrication facility. The APL COB process is...
implemented with conventional printed wiring board technology and does not require high-cost ceramic substrates. The substrate has ten layers: eight signal layers, one power layer, and one ground layer. Circuit interconnects on each layer use tracks that are 5 mils wide with 5-mil spaces between tracks. Interconnects between layers use through-hole vias with 25-mil pad and 10-mil hole feature sizes.

Conventional circuit board design tools were used to develop the substrate design. Bond pads for bare dies were manually placed and connected to vias. The tracks were then auto-routed, with a greater than 99% completion rate. The board has 2335 tracks and 3934 vias. One side of the board has all the bare die components, and the other side has conventionally packaged parts. This approach simplifies the handling of the module.

The COB process allowed high-power dissipation components to be used without heat sinks. High-power MIL-STD-1553 transceiver components were mounted as die directly on the board. Thermal vias and planes on signal layers provided an adequate heat path from the die to the board, and then across the board to the module frame. This contrasts with conventionally packaged designs that require additional heat sinks because the transceiver package itself increases the thermal resistance, making it more difficult to remove heat from the die.

Under this ATD project, the drawings for the RTX2010 module were completed and two of the modules were fabricated. One of the modules was electrically tested and is currently undergoing thermal cycling in air. Engineering support modules were fabricated to connect power and ground to the RTX2010 module through the stackable connector. Three Actel FPGA/snapstrate assemblies were required for each RTX2010 module. Each assembly was constructed by bonding an FPGA die to a snapstrate carrier, wirebonding the FPGA die pads to the pads on the snapstrate, and then covering the die and wirebonds with a protective epoxy coating. FPGA die were programmed by soldering temporary wires to the outer edges of the snapstrate and connecting the wires to a pin grid array (PGA) adapter. The PGA adapter was inserted into an Actel programmer and the FPGA was programmed as if it were a standard PGA component. After programming, the edges were removed from the snapstrate, leaving a final assembly that is only slightly larger than the bare die itself. The snapped snapstrate has wirebond pads around its periphery. Each snapstrate was bonded to the module substrate with nonconductive epoxy, and the snapstrate pads were wirebonded to pads on the board.

During bench-level testing, a short circuit between a signal line and ground was discovered, but no visible defects could be identified. After determining which track on the board corresponded to the shorted signal, 30 mA of current was injected into the track. The short was located in a defective die component with the use of thermal scanner. The temperature of the defective die increased by about 5 °C above ambient. The defective die was removed and a new die was epoxied and wirebonded to the board. The RTX2010 module then functioned correctly. This demonstrated the repairability of APL’s COB process.

The RTX2010 module incorporates several miniaturization technologies, including COB, stackable connectors, miniature input/output connectors, die with small pitch bond pads, ceramic substrate mounted die, and infrared communications. It serves as an excellent technology validation vehicle. This validation has increased the Technology Readiness Level of the COB process and will allow the technology to be readily inserted into future spacecraft programs.
In order to scale down the size of high-voltage circuits without encountering breakdown and coronal discharge problems that can seriously damage instruments' electronics systems, the ATD project investigated advanced techniques necessary to design miniature high-voltage circuits. We investigated the behavior of high-voltage circuit designs with respect to changes in dielectric and conductive materials, conductor lengths and shapes, and the topologies of ground planes.

The High-Voltage Power Supply ATD project included two separate tasks:

1. Study the basic behavior (corona) with different circuit configurations to evaluate the minimum spacing between lines and the effect of ground plane, conductor shapes, dielectric properties, and cutouts.

2. Design and develop the miniaturized Cockcroft-Walton voltage multiplier circuitry, using the results from task 1.

We initially reviewed the literature on high-voltage breakdown phenomena in vacuum, identified nonconductive substrates for a high-voltage test coupon, and performed the electrostatic analysis of various circuit configurations to determine the optimum layout. The electrical and mechanical stress points in the power supplies were also investigated. We then demonstrated the applicability of the new technologies by building and evaluating the high-voltage section of a high-voltage power supply. A high-voltage test facility was used to perform the high vacuum breakdown tests on the coupons.

The ATD project concentrated on using the dielectric properties of materials that would minimize breakdown and on designing and fabricating test samples using the various packaging techniques in order to provide quantitative measurements of their performance. We identified and evaluated electronics components that are best suited for use in high-voltage power supplies and in the distribution and filtering of high voltages within instruments.

Test coupons with conductor spacing varying from 0.125 to 5.0 mm were made with ceramic and polyimide-glass substrates to measure the corona initiation voltage at different levels of vacuum. Several tests by industry have been made only in a semi-vacuum environment; none of those tests cover the hard vacuum (500-km altitude and higher) that would support satellite application. Industry's test reports indicated that there is “no difference” in the corona initiation...
voltages between sharp points, rods, and parallel plates at 43-km altitude. One interesting note is that potting with Uralane is much more difficult than with other materials because of its faster curing cycle. Material with a faster curing cycle may have unwanted voids, and it is very difficult to analyze and control the behavior of voids in high-voltage design.

We used four basic coupon designs using polyimide and ceramic substrates:

- Design 1: Circuit patterns have no slot and no ground plane.
- Design 2: Circuit patterns have slots and no ground plane.
- Design 3: Circuit patterns have slots and ground plane.
- Design 4: Circuit patterns have no slot and have ground plane.

We performed the corona initiation voltage measurements for these designs under hard vacuum (for 500-km altitude and higher). Test samples had both potting and without potting configurations. We believe that the test results from the potting study will help us in the future to define high-voltage power supply characteristics. We selected three coating/potting materials: no coating (for a reference sample), Parylene, and Uralane.

Further, the ATD project identified and evaluated components for a Cockcroft-Walton voltage multiplier. Design and fabrication of the Cockcroft-Walton substrates were completed with three units populated with parts. Two of the units were coated with a Parylene dielectric coating, and the third was uncoated. The breakdown characteristics of the coated and uncoated units were similar in vacuum. Neither unit exhibited a voltage breakdown until 8 kV.

A Spice analysis of the Cockcroft-Walton circuit was conducted to model the operational characteristics of the unit, e.g., the turn-on transients, the voltage stress across each component, and the output impedance of the unit and the output voltage as a function of input wave shape.

![Spice analysis of the Cockcroft-Walton multiplier. Drive voltage = 55 V @ 100 kHz; output voltage = 3800 V; output impedance = 1.2 MΩ.](image)
Traditional spacecraft power systems incorporate a solar array energy source, an energy storage element (battery), and battery charge control and bus voltage regulation electronics to provide continuous electrical power for spacecraft systems and instruments. Dedicated power converters condition power for individual loads and provide limited fault isolation between systems and instruments, while a centralized power-switching unit provides spacecraft load control. Protection of the spacecraft battery from under-voltage conditions that can result in battery cell failure typically depends on hardware fault detection to alert the spacecraft processor, which removes fault conditions and noncritical loads before permanent battery damage can occur.

Cost-effective operation of a micro-sat constellation requires a fault-tolerant spacecraft architecture that minimizes on-orbit operational costs by permitting autonomous reconfiguration in response to unexpected fault conditions. We have developed a new micro-sat power system architecture that enhances spacecraft fault tolerance and improves power system survivability by continuously managing the battery charge and discharge processes on a cell-by-cell basis. This architecture is based on the Integrated Power Source (IPS), which integrates dual-junction solar cells, lithium ion battery cells, and processor-based charge control electronics into a structural panel that can be deployed or used to form a portion of the outer shell of a micro-spacecraft.

The first-generation IPS is configured as a 1-inch-thick (2.5-cm-thick) panel in which prismatic lithium ion battery cells are arranged in a $3 \times 7$ matrix (26 VDC) and a $5 \times 1$ matrix (3.7 VDC) to provide the required output voltages and load currents. A multi-layer structure holds the battery cells as well as the individual thermal insulators that are necessary to protect the lithium ion battery cells from the extreme temperatures of the solar cell layer. Independent thermal radiators, located on the back of the panel, are dedicated to the solar cell array, the electronics, and the battery cell array. In deployed panel applications, these radiators maintain the battery cells in an appropriate operational temperature range. In body-mounted panel applications, solar array and battery heat are independently routed to remote radiators.

The IPS electronics sense the instantaneous charge current, cell voltage, and temperature of each battery cell and use that information to control the charging process. The electronics include a processor that sets the charge current for each string of cells in the battery matrix and controls individual cell bypass currents to implement the control algorithms and maintain

**IPS solar cell panel assembly at NASA Glenn Research Center with dual junction cells from EMCORE.**

*I* NASA Glenn Research Center.

**Autonomous Integrated Power Source Architecture**

*Paul Schwartz, Al Hepp, * Binh Le, Ark Lew, Sharon Ling, Mike Piszczor, * Dave Stott, Joe Suter, and Bruce Williams*
charge state equilibrium in the absence of precisely matched battery cell characteristics. The charge current for a string with a failed battery cell can be set to zero, leaving the full solar array current available for operational battery cells. The charge control processor can be programmed to permit virtually any flight-qualified battery chemistry to be used and can recognize and correct battery cell conditions that may lead to cell failure or reduced cell life. The processor continuously generates a coulometric record for each battery cell, which provides critical information for spacecraft energy balance based autonomous control algorithms.

The IPS provides unregulated voltages that can be distributed to spacecraft systems and instruments in a traditional manner or used to power dedicated spacecraft loads through linear regulators or power converters. Critical and noncritical spacecraft loads can be powered from independent power sources, further improving spacecraft fault tolerance and reducing micro-sat constellation operational costs. In addition, eliminating the shared power lines between spacecraft systems and instruments eliminates the conducted power line noise coupling that is typical of traditional architectures. Spacecraft integration testing can be simplified by eliminating portions of the traditional set of integration tests.

This ATD effort focused on developing the electrical, mechanical, and thermal designs required for a multi-purpose, deployed micro-sat power panel. The solar cell component layer, which was developed at the NASA Glenn Research Center, consists of dual-junction solar cells that are approximately 21% efficient. The battery layer was implemented using prismatic lithium ion cells for the high-voltage matrix and thin, state-of-the-art, solid electrolyte lithium ion polymer cells for the low-voltage matrix. The electronics were designed using a radiation-tolerant micro-controller and flight-qualified components for the data-gathering circuitry and the string current and cell bypass shunt electronics. Proper operation of the string current and cell bypass current control electronics was verified by simulation.

One of the most challenging aspects of the ATD IPS development was maintaining the battery cells in an appropriate operational temperature range for both full Sun ($\beta = 90$) orbits and orbits in which the Sun vector is in the orbit plane ($\beta = 0$). Simulation results confirm that the current IPS design will maintain proper battery cell temperature for all low Earth orbits. Simulation results for the $\beta = 0$ orbit under worst-case hot conditions are shown.

A prototype IPS panel has been fabricated and assembled as part of the ATD effort. IPS development tasks that remain to be performed include electrical testing of the prototype, development of the charge control algorithms and software, and flight qualification of the prototype unit. U.S. and international patents have been granted for the IPS concept, and a U.S. patent has been granted for the IPS electronics architecture.

http://sd-www.jhuapl.edu/ATD_NASAAPL/
The goal of this ATD program was to dramatically lower mass, power, and cost for spaceflight nonvolatile memory while maintaining flexibility to upgrade memory capacity by using commercially available laptop and camera mini- and micro-disk drives in a flight standard package. With a standard packaging design, we could hold future development costs to very low levels for individual missions as well as accommodate future upgrades in commercial disk drive performance capability. This ATD project achieved significant reductions in total mass, power, and cost for comparable high-density high-read/write capabilities over current solid-state flight data storage components.

Laptop and digital camera disk drives with storage capacity of 340 MB to 1 GB have reached the level of ruggedness required for spaceflight. This ATD program focused on device testing and development of a flight enclosure to hermetically package the drives. It considered long-duration vacuum seal, launch loads, momentum compensation, thermal issues, materials, electrical and mechanical spacecraft interfaces, and radiation hardness and shielding at minimal mass and volume. This project developed such an enclosure. The total package can withstand standard launch and spaceflight environments. It has a 680-GB storage capacity (dual, momentum-compensated, IBM 340-GB micro-drives) in a 128-g package (total mass), with a sustained data rate of 4.2 MB/s, and standby and write currents of 65 and 300 mA at 3.3 VDC supply (0.2 and 1 W, respectively). Under standby conditions, the total dose radiation hardness capacity was between 20 and 30 krad. This disk drive and packaging concept compares favorably with a current NASA mission solid-state recorder with 312-GB capacity, data rate of 3.8 MB/s at 4 W read/write (1 W standby), and 450 g mass.

We began by considering the mechanical integrity of micro-drives for launch environments to determine intrinsic ruggedness vs. potential need for specialized shock-mounted enclosure design. This inherent ruggedness was proven by testing the commercial disk drives for shock and vibration. An IBM 340-GB micro-drive was directly shaker mounted and subjected to sine burst and random test levels followed by read/write cycles to determine survivability. The drive was tested to levels above those typically encountered on board-mounted components for typical spacecraft programs. Full qualification level three axes of testing were performed with no anomalies, thereby indicating we could ignore shock mitigation mounting techniques and proceed to board-level packaging design and fabrication and subsequent package-level vibration and thermal-vacuum testing. We focused on a housing for two IBM 340-GB micro-drives (back-to-back for momentum
compensation), including package sealing and typical spacecraft interfaces such as Small Computer Standard Interface (SCSI). The mechanical mounting requirements for the disk drive initially appeared to dictate the use of Cotherm between the drive and the bracket to ensure good conductive heat transfer to the chassis for conduction into the spacecraft but no other shock mounting.

The housing and mounting system was analyzed for stress and shock. We then reviewed the target drives selected, selected connectors, and more thoroughly investigated the drive finalists. Early in the design process, we decided against a large (9-GB) drive and concentrated on the more miniaturized (camera) version. Announcements from IBM about the performance leaps of micro-drives in the 340-MB range for less than 16 g appeared to make direct competition between the micro-drives and solid-state recorder boards a real possibility and well within the scope of this ATD effort. IBM 340-MB drives and connector adapters for board mounting and testing were procured after evaluating disk drives from IBM and Hewlett Packard. Subsequently, design and fabrication of all components (board, housing, seals, connectors, etc.) was completed, including assembly and potting. After final mechanical and thermal-vacuum testing, total dose level radiation testing was performed.

Total dose radiation for current complementary metal-oxide semiconductor (CMOS) integrated circuits has a dramatically greater effect when the device is powered. Unfortunately, it was not possible to operate the micro-drive in the chamber over long cables. Nor was it feasible on this budget and schedule to build radiation-hardened electronics to operate the drive in the chamber. Since the drive was not operating in read/write, it was unlikely that all internal circuitry was powered. The 25 mA consumed was in line with the published standby current for the device, but significantly lower than the 250-mA operational current. Our test, therefore, set an upper bound on the total dose limit (i.e., it could fail at a lower total dose if operating).

We applied power only to one drive and monitored its current while it was exposed to the radiation. Periodically we removed the drives from the chamber and tested both in a laptop PC. We expected to see the drive current increase with radiation exposure, with an eventual sharp increase. Although we did see an increase in current, we did not see a dramatic jump when the drive failed. This is likely because the current was not dominated by a single integrated circuit but was composed of a comparatively high standby current from several integrated circuits, only one of which failed. It could also be caused by failure modes that we are not familiar with but that have been seen in newer, smaller geometry integrated circuit processes.

We also saw the unpowered drive fail at a total dose fairly close to the powered drive. This also leads to the possibility that the failure occurred in a normally unpowered portion of the drive. The increase in current occurred at about 20 krad, which is an acceptable total dose for many programs, especially if that can be improved by shielding. Total dose testing was performed first because it was most affordable. This testing is probably valid for a mission during which the drive is unpowered most of the time. If the drive were to be operating often, a total dose test with an operating drive would be needed. Single event upset (SEU) testing is more difficult, but several new test facilities might be able to provide this without IBM bare die.

In summary, all testing to date indicates that the IBM commercial micro-drives as enclosed have promise for spaceflight and are highly competitive with current solid-state recorders for mass, power, storage, and data rate at significantly reduced cost.
A significant challenge in the advancement of scientific spacecraft for NASA is the improvement of the radio-frequency (RF) communications capability on board the spacecraft. The performance of the RF communication system has a first-order impact on the science return of the mission. The Communications Thrust Area has focused on three key technology areas that we feel can contribute significantly to future NASA space science missions: (1) high-bit-rate communications, (2) advanced transceiver systems, and (3) ultrastable, low-profile quartz resonators. The technologies in these areas address both near-Earth and deep-space missions. In this report we review the technology areas and discuss the specific project accomplishments in each area. We also identify where some of the work has been infused into flight programs or has generated continued sponsorship.

High-Bit-Rate Communications

Because of fundamental laws of physics and communication theory, the science return of a spacecraft mission can be increased in only a limited number of ways. On board the spacecraft, we can increase the transmit power, increase the antenna gain, incorporate error correction coding, or operate at a higher microwave frequency. The last technique assumes that the communication system incorporates antennas of fixed aperture area at both ends of the link.

Because small spacecraft are limited by their size and cost, it is advantageous for them to use solid-state power amplifiers (SSPAs) at low-to-moderate RF output power levels ($\leq 20$ W). The design of microwave SSPAs is an exacting art that requires a combination of analytical skill, experimental skill, and state-of-the-art measurement facilities. As part of the ATD effort, we have focused on developing and characterizing X- and K$_a$-band power amplifiers and phase shifters for phased array applications. In addition to the hardware produced, this effort has contributed significantly to the space science community by creating a world-class capability in power amplifier research and development at APL.

Increasing the size of a spacecraft high-gain antenna has a first-order effect on the science return of the mission. However, the size of the spacecraft antenna is limited by the mass margin of the mission and the size of the launch vehicle fairing. A classic approach to this problem is the use of an inflatable antenna. However, despite their promise, inflatable antennas have not been incorporated into space science missions to date because of the fear of an inflation failure. To address this problem, we have developed a hybrid inflatable antenna that combines a reliable rigid reflector with an inflatable annulus to greatly increase the antenna size on orbit. This technique provides a high-gain backup even in the event of an inflation failure, thereby avoiding the “all or nothing” problem commonly associated with inflatables. We hope that this new, innovative concept greatly accelerates the incorporation of inflatable antennas into future space science missions.

Another problem with high-gain antennas is that they must be pointed precisely at the Earth. This is accomplished by either moving the spacecraft, using a gimbal, or scanning the antenna electronically. Under the ATD program, we have focused on a simple, low-cost technique for achieving one-dimensional electronic scanning using an array of slotted waveguide “sticks.” This approach is both rugged and low cost; however, the slots must be cut into the narrow wall of the waveguides, resulting in a design that is inherently linearly polarized. This results in a 3-dB loss when the...
antenna is used in conjunction with the circularly polarized antennas at the Deep Space Network. Surprisingly, despite over 50 years of research and development of waveguide technology, a simple solution for achieving circular polarization directly from the narrow wall of the waveguide has never been achieved. Under the ATD program, major progress has been made toward solving this problem, and the knowledge gained has been infused into the MESSENGER flight program with the potential of doubling the science return of that program.

**Advanced Transceiver Systems**

Many of the emerging scientific satellite missions require either small satellites or constellations of extremely small satellites commonly referred to as "microsats" or "nanosats." These missions have generated the requirement for miniature, low-power RF transceiver systems on board. A challenge is to develop these systems without incurring the high development and production costs commonly associated with custom microwave integrated circuits.

Under the ATD program, we have developed a very low-power (~1.5 W) digital receiver to address the needs of future microsat missions. The architecture can be scaled to enable operation at either S or X band on both near-Earth and deep-space missions. The targeted footprint size is 4 × 4 inches (10 × 10 cm). Leveraging off high-technology advances in the wireless world, this receiver is easy to fabricate, resulting in costs that are lower than those for conventional hardware flown on NASA missions.

**Low-Profile, Ultrastable Oscillator Technology**

The requirement for excellent frequency stability is an important but often overlooked ingredient in the design of a communication system. The radio science community has depended for years on the availability of frequency sources with excellent long-term frequency stability and low phase noise for their measurements. In the space telecommunications world, low phase noise is required for generation of microwave signals in the K$-$band region and for low-bit-rate downlink communications. All of these requirements have typically been met with the world-class ultrastable oscillators (USOs) produced by APL over the years. However, USOs have historically been relatively large because of the need to thermally stabilize a bulky quartz resonator. In addition, the cost of the USO is often high because a large number of expensive resonators must be purchased and screened due to a low yield of high-performance units that meet the mission requirements. Under the ATD program, we have addressed these problems by developing a brazed quartz resonator suitable for packaging in a low-profile ceramic enclosure. The results of this project are an important step toward the routine incorporation of low-profile, less-expensive USOs into communication and radio science systems.

**Technology Transfer**

All of the technology development in the Communications Thrust Area has been conducted with technology transfer in mind. The role of APL as a research and development organization is to develop technology that will benefit the nation and the space program as a whole. Technologies such as the K$-$band phased array components, the hybrid inflatable antenna, and the low-profile quartz resonator have been developed through corporate partners who can make them available to the space community. Other products, such as the $S/X$-band low-power digital receiver, can be made available to industry through the technology transfer mechanisms at APL.
High-Bit-Rate Communications

K\textsubscript{s}-Band MMIC Phased Array Components

John E. Penn

Satellite communications have evolved to higher and higher frequencies as communication rates and requirements have increased. NASA’s Deep Space Network (DSN) is used to communicate with spacecraft across the solar system. NASA is working to advance the DSN’s communications capability from X band (about 8 GHz) to K\textsubscript{s} band (about 32 GHz). The main reason for increasing the communication frequency is to achieve higher data transmission rates for the same transmitted power level. With all other parameters held constant, a K\textsubscript{s}-band system would provide 16 times as much data as an X-band system. In practical application, a data-rate improvement factor of 4 can be achieved. Bandwidth availability is also increased by the switch from X band to K\textsubscript{s} band. For a spacecraft in deep space with limited power resources for communications, it is easy to see why there is an interest in increasing the science return by going to K\textsubscript{s} band. However, designing efficient power amplifiers at K\textsubscript{s} band is considerably more difficult than designing at X band because of the close tolerances involved and the lower efficiencies of the devices.

Given that microstrip and connector losses tend to be higher at K\textsubscript{s} band, one way to improve amplifier efficiency in a phased array is to use spatial combining, which is extremely efficient compared to lossy combiner networks. Many small, highly efficient K\textsubscript{s}-band amplifiers can be combined in a large phased array, resulting in a system that degrades gracefully with amplifier failures and provides a combined radio-frequency (RF) power equal to the sum of the individual elements. Two key components in a phased array are the power amplifiers and the phase shifters, which allow the focused beam pattern to be steered.

Under the ATD program, we have designed and built custom microwave monolithic integrated circuits (MMICs) to provide the functions of a K\textsubscript{s}-band power amplifier and a K\textsubscript{s}-band 4-bit digital phase shifter. In a phased array design, these two components are critical. Power amplifier MMICs at 32 GHz are difficult to find, and those that are available are not very efficient. We have designed a 32-GHz MMIC power amplifier and completed first-pass fabrication at the TriQuint/Texas foundry. The first-pass results are very good (Table 1); a power-added efficiency of nearly 30% was achieved.

Table 1. K\textsubscript{s}-band MMIC power amplifier goals vs. performance (first foundry pass).

<table>
<thead>
<tr>
<th>Gain (dB)</th>
<th>Power Out (dBm)</th>
<th>Power-Added Efficiency (%)</th>
<th>Voltage (V)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>12–14</td>
<td>27</td>
<td>30</td>
<td>6–8</td>
<td>Goals (optimized at 32 GHz)</td>
</tr>
<tr>
<td>14–15</td>
<td>&gt;27</td>
<td>28–29</td>
<td>6–8</td>
<td>Measured (30 GHz)</td>
</tr>
</tbody>
</table>

The K\textsubscript{s}-band solid-state power amplifier, which was designed under the ATD program, produced a 29% power-added efficiency (PAE).
states, accuracy of phase shifts, total insertion loss of the phase shifter, and bandwidth. During the design of the 4-bit phase shifter, different topologies were explored for each of the 180-, 90-, 45-, and 22.5-degree bits. Trade-offs of the various topologies appropriate to each phase shift bit were performed to minimize insertion loss imbalance, reduce total insertion loss, and provide accurate wideband phase shift. The nominal 22.5-degree bit used a Lange coupler with a tuned switched reflection for a wideband 22.5-degree phase shift. A much smaller alternate 22.5-degree “FET” bit used a differential phase shift from two FETs with opposite gate control voltages to provide broadband phase shift. The alternate 22.5-degree topology was small and provided excellent results. Accurately predicting phase at K\_b band is generally much more difficult than estimating insertion loss. Agilent’s EEsOf simulator was used for much of the initial design process, and electromagnetic simulators like Sonnet and Ansoft’s High-Frequency Structure Simulator were used to provide a more accurate analysis of the best design candidates.

We have completed first-pass fabrication of the 4-bit \(K\_b\)-band phase shifter at the TriQuint/Texas foundry. The results (Table 2) are very promising. More design work and a second foundry pass will be required to optimize the design.

### Power Transistors for Highly Efficient X-Band Solid-State Power Amplifier Development

**Perry M. Malouf**

As part of our high-bit-rate communications initiative, we characterized state-of-the-art transistors for applications in X-band (8.4-GHz) power amplifiers. To minimize spacecraft power consumption, it is desirable to maximize the power-added efficiency of the amplifier design. Commercially available transistors were tested, including ones from the TriQuint Semiconductor product line of heterojunction field effect transistors (HFETs) and pseudomorphic high electron mobility transistors (pHEMTs). Each type

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**Table 2. \(K\_b\)-band MMIC phase shifter preliminary results at 32 GHz (first foundry pass).**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Phase Shift</th>
<th>Insertion Loss Balance</th>
<th>Insertion Loss (dB)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>180°</td>
<td>170</td>
<td>0.1</td>
<td>~3</td>
<td>Measured as a single bit</td>
</tr>
<tr>
<td>90°</td>
<td>104</td>
<td>~3*</td>
<td></td>
<td>Measured in overall 4-bit configuration</td>
</tr>
<tr>
<td>45°</td>
<td>68</td>
<td>~0.7</td>
<td></td>
<td>Measured in overall 4-bit configuration</td>
</tr>
<tr>
<td>22.5°</td>
<td>35</td>
<td>0.5</td>
<td>1.0–1.5</td>
<td>Measured as a single bit</td>
</tr>
<tr>
<td>22.5° FET</td>
<td>23</td>
<td>~0.2</td>
<td>1.0–1.5</td>
<td>Measured as a single bit</td>
</tr>
</tbody>
</table>

*The cause of the high insertion loss balance is being investigated.
FET = Field effect transistor implementation.
The gain (upper) and power-added efficiency (lower) of several power amplifier circuits is shown, each containing a different kind of commercially available, state-of-the-art power transistor. The circuits were evaluated under like conditions so that the performances of the various transistors could be accurately compared.

An important part of this effort involved the use of a microwave load/source-pull measurement system. Such a system facilitates the optimization of amplifier performance by allowing independent adjustment of the impedance seen by the load and source ports of the transistor. The need to design and build multiple circuits with different matching networks is obviated because the best design is found relatively quickly by measuring one test circuit. The same capability may be easily applied to other state-of-the-art devices as they become available, and may be applied to circuit design at other frequencies including K_a band.

During the course of the ATD program, APL acquired a highly capable load/source pull system. This system, which can operate over 0.8 to 40 GHz, was used to great advantage in this ATD effort to characterize and understand the performance of microwave power transistors. Each tested circuit consisted of the transistor under test, quarter-wave step transformers at the ports of the transistor, bondwires, and a 50-Ω microstrip for the input and output lines. Extensive testing revealed that the impedance matching at the transistor ports is very sensitive to bondwire inductance. For some circuits, the bondwires were carefully configured to obtain the required inductance. All circuits were evaluated in the load/source-pull system under the same set of test conditions.

A representative summary of measurements in the accompanying figure illustrates the measured gain vs. input power and the power-added efficiency vs. input power of various transistors. These plots facilitate the comparison of performance between the transistors that were tested. The 4.8-mm gp HFET device demonstrated the highest power-added efficiency. This device has subsequently been selected for use in developing a highly efficient solid-state power amplifier on the MESSENGER flight program.

K_a-Band Hybrid Inflatable Dish Antenna

Cliff E. Willey, Robert S. Bokulic, William E. Skullney, and Ron C. Schulze

Inflatable antennas are the subject of current space research because of their potential for enabling high-bit-rate communications. However, a significant problem associated with inflatable technology is the “all-or-nothing” scenario, where the success of the mission depends on successful deployment of the antenna. For this reason, the application of inflatable antennas is currently limited mainly to missions where a very large aperture is needed to enable the mission. Examples of such missions include interstellar
probes and large imaging radar satellites. The ATD program is developing a new inflatable antenna concept that can be integrated into spacecraft missions on a much shorter time scale than would be possible with other inflatable antenna approaches.

This concept might be applied to a typical 1-m dish to increase its diameter to 4 m or more. An inflated 4-m flight antenna could return a bit rate on the order of 1 Mbps from Mars with a 30-W Kₗ-band amplifier. A major challenge is achieving a reflector accuracy on the order of ±0.5 mm to ensure proper operation at Kₗ band.

Our current ATD activity is a collaboration between APL and ILC Dover Corporation. Our work has focused on the construction of a breadboard hybrid inflatable antenna. This breadboard, being built by ILC Dover for the ATD program, will be a 2-m-diameter parabolic dish designed to demonstrate that the surface accuracy required for Kₗ-band operation can be achieved. It consists of a 0.5-m-diameter rigid reflector surrounded by a 2.0-m-diameter inflatable annulus. Upon inflation, the shape of the annulus will be precisely measured using optical measurement techniques. From these measurements, we will be able to determine the errors between the inflated surface and the tooling used to create it. We will also be able to project the radio-frequency (RF) efficiency of the dish. While we have made significant progress on designing, developing, fabricating, and testing this new antenna concept within the ATD program, continued development is needed. Follow-on work is required in the areas of RF feed development, rigidization techniques, and thermal testing.

A concept has been developed under the ATD program for a hybrid approach that avoids the “all-or-nothing” scenario by providing a backup capability in the event of an inflation failure. This antenna combines a fixed parabolic dish with an inflatable annulus to greatly increase the reflector size on orbit. The fixed parabolic dish provides a “risk buffer” whereby a high-gain capability is retained even in the event of an inflation failure. A dual feed ensures operation of the smaller fixed dish throughout the mission. The inflatable annulus is stowed compactly under the fixed dish to fit a variety of spacecraft and launch vehicle envelopes. Moderate gas pressure deploys the annulus, which forms a parabolic reflector surface.

Shortly after inflation, the composite materials that form the annulus surface are made rigid by thermal, ultraviolet, or other curing methods.

Hybrid inflatable antenna in its deployed configuration. This concept avoids the “all-or-nothing” problem commonly associated with inflatables.
Circularly Polarized Slotted Waveguide Arrays

Robert K. Stilwell

Spacecraft often require high-gain, narrow-beam antennas to support high-bit-rate communications at long ranges. These antennas must be accurately pointed toward the ground antennas to function. If the antenna is rigidly mounted to the spacecraft, the spacecraft structure must be oriented to support the communications, often resulting in unfavorable conditions for the instruments and the power and thermal control systems. A mechanically gimbaled antenna can be pointed independently of the spacecraft, but at the expense of cost, complexity, weight, and impact on the spacecraft configuration. In some missions, the spacecraft can be easily moved in one dimension (rolled, for example) during periods of contact with Earth. In that case, an antenna that can be scanned in the other dimension can be used to point a beam toward Earth. This portion of our ATD effort addressed one-dimensional electronically scanned antennas for that type of application.

For deep-space missions, a one-dimensional scanning array antenna should operate at the frequencies supported by the Deep Space Network (DSN) ground stations, be circularly polarized, have high aperture efficiency and low loss, and have a robust construction but be lightweight. An example of an antenna meeting most of these requirements is an array of waveguide “sticks.” Each stick is itself an array of slot radiators. The individual sticks can be fed by transmit modules containing power amplifiers and phase shifters. The phase shifters are used to steer the beam in the plane orthogonal to the axis of the waveguides. The slots of a single stick radiate in phase to produce a narrow broadside beam in the other plane. The major drawback of the slotted waveguide design is its linear polarization. If circular polarization can somehow be achieved without affecting the strong advantages of the basic concept, the downlink data rate can be increased by a factor of 2. One goal of the ATD effort was to develop a method to achieve circular polarization from a slotted waveguide array that could scan at least ±45 degrees. This technology would not only be useful for the one-dimensional scanning scenario, but might also be used in other applications, such as medium-gain fanbeam antennas.

A number of concepts for achieving circular polarization were considered. They are illustrated in the accompanying figure. Concept A uses specially shaped slots to generate circular polarization. As part of our work, a simplified transmission line model with distributed current source excitation was developed to model such slots. A fundamental limitation with this approach was discovered in the process. In a typical slotted waveguide array, the radiating slots are separated by one-half of a waveguide wavelength and must have a way to achieve “phase reversal” to compensate for the resulting alternating 180-degree change in excitation. For narrow-wall slots radiating a component with their electric fields normal to the waveguide axis (which is required for circular polarization), there is no...
way to obtain this phase reversal. Circularly polarized slots must therefore be separated by a full waveguide wavelength, producing subsequent problems with grating lobes and loss of directivity. Finite element modeling demonstrated that these problems would destroy the advantage obtained from achieving circular polarization.

Concept B uses a single-layer polarizer and a conventional linearly polarized slotted waveguide array. The polarizer, like that studied by Kyeong-Sik Min of the Tokyo Institute of Technology and his associates, consists of an array of parasitic dipoles located a small distance above the waveguide slots. Our work using numerical modeling and experimental work indicates that this approach can be developed to achieve good circular polarization when the beam is scanned normal to the array face, with some degradation expected as the beam is scanned to 45 degrees. The mechanical configuration may, however, be a problem for some spacecraft applications. The parasitic dipoles are typically fixed to a dielectric substrate that must be accurately positioned relative to the waveguide array. A layer of low-density foam is a convenient way to do this. For high-temperature environments, significant materials problems can be encountered with both the dielectric substrates and the foam spacers.

Concept C was devised to avoid the materials problems of the dipole polarizer. A conducting plane placed in front of a waveguide array will have regions of high current midway between the waveguide slots. Crossed slots cut into the conducting plane will couple to these currents and can be dimensioned to radiate circular polarization. An “all-metal” structure is conceivable, which will avoid high-temperature materials problems. Experimental work with this configuration confirmed that good circular polarization can indeed be generated. However, there is a problem with unwanted energy propagation in the region between the waveguide sticks and the conducting plane of the polarizer. If the energy propagation is not controlled, the circularity of the radiated field is seriously degraded and strong mutual coupling among the waveguide sticks is to be expected. Microwave absorber was used in the experiments with a single stick, but significant energy was lost in the process. The crossed slot polarizer will require the development of an efficient way to control energy propagation under the polarizer plane.

The knowledge gained from this ATD work has been infused into the MESSENGER spacecraft design and has the potential to double the science return from that mission. The MESSENGER spacecraft will orbit the planet Mercury and must at all times remain protected from the solar energy by a sun shade. The spacecraft is, however, free to rotate about the spacecraft–Sun line, so a one-dimensional electrically scanned antenna system can be used in conjunction with the attitude control system to point a beam toward the Earth. Concept D uses inclined monopole elements mounted directly to the waveguide in an all-metal structure. The monopoles are excited parasitically from the waveguide slots and provide the radiated field component required to produce circular polarization when combined with the fields from the slots. Experimental work with this concept has demonstrated good circular polarization, tuning characteristics, and bandwidth.
Advanced Transceiver Systems

Wesley P. Millard, Robert S. Bokulic, Daniel J. DeCicco, Sheng Cheng, John E. Penn, Hollis H. Ambrose, and Robert F. Platte

New exploratory space missions proposed by NASA are creating the need for smaller, more efficient spacecraft that fly either individually or as part of a constellation. These new requirements have led to the design of the next generation of spacecraft called “microsats” and “nanosats.” The new spacecraft require systems that operate at low power, are small, and cost a fraction of the systems currently produced.

This project within the ATD program has focused on an advanced S/X-band digital receiver that is designed to meet the communication needs of the next generation of spacecraft (Table 1). The new receiver possesses a small form factor and a very low power design. The key to these performance improvements is the use of commercially available highly integrated components. Over the past decade, the commercial world has made many advancements in fabrication processes and in the level of device integration. These high-technology developments have led to the mass production of highly integrated, high-speed, very-low-power devices. The advanced S/X-band digital receiver uses these new commercial monolithic integrated circuit products to create a system that is low enough in both power and cost to be “microsat” compatible.

The architecture for the advanced system incorporates a two-stage heterodyne receiver. The design incorporates both analog and digital systems. In the absence of an uplink carrier signal, most of the high-speed digital circuitry, such as the command detector unit and ranging, is inoperative. Only the circuitry essential for achieving carrier lock is active. Once the low-power digital phase-lock loop (PLL) has acquired lock, the remaining digital systems are powered to enable normal communications. This switching feature, combined with the analog subsystems described subsequently, enables the overall receiver system to consume much less power than other types of space receivers currently in use.

The first mixer of the down-conversion chain is an active image rejection mixer. Its innovative design allows low-power, low-noise mixing to occur at either S or X band, depending on the local oscillator frequency. The local oscillator signals are generated from a fractional-N frequency synthesizer. This synthesizer is a highly integrated digital design that is currently used in many commercial wireless communication products. The synthesizer subsystem generates the necessary local oscillator frequencies with minimal power consumption. The remainder of the down-conversion chain is implemented with standard, high-impedance, wireless components that add up to 160 dB of voltage gain.

The active image rejection mixer operates at both S and X bands.
One custom monolithic microwave integrated circuit (MMIC) was designed for the advanced receiver system to minimize power. It is an X3 frequency multiplier, designed by APL and fabricated by TriQuint Semiconductor. The multiplier is used to convert the S-band synthesizer output to X-band frequencies. It consumes only 125 mW of power as compared with commercially available multipliers, which consume about 1.4 W.

The digital PLL of the receiver system is programmed into a field programmable gate array. This implementation method not only reduces power compared to an analog PLL but also reduces design and simulation time. Eventually the automatic gain control, ranging, command detector unit, two-way noncoherent Doppler tracking, and other computation blocks will be implemented in the same manner.

During the ATD program, the advanced receiver system was designed, built, and tested as an X-band breadboard receiver. The breadboard includes four evaluation test boards made by commercial integrated circuit manufacturers and four boards designed in house. Each subsystem was assembled and individually tested for noise, power consumption, and performance. The final designs for all of the subsystems in the receiver meet or exceed their intended functional and physical requirements (see Table 2 for power performance). From this point, the subsystems were assembled to form a carrier tracking loop. Once the design was finalized, a unified schematic and layout were compiled for the receiver, excluding the digital subsystem. An analog board for the receiver has been built on one side of a 4 x 4 inch (10.2 x 10.2 cm) printed circuit board, leaving plenty of room for the digital subsystem on the back side for later prototypes.

In summary, this project has developed a very low-power digital S/X-band receiver for future microsat applications. We have built and tested a breadboard version to demonstrate the ability to lock to an X-band signal, and have built a first-cut version of a 4 x 4 inch analog board. A complete summary of the project accomplishments follows:

- Produced a flexible design capable of operation at either S or X band
- Designed, built, and tested a breadboard receiver
- Met low power requirements (≤1.3 W)
- Fabricated a small 4 x 4 inch (10.2 x 10.2 cm) prototype board
- Designed and built a multi-band image rejection mixer
- Designed and built a low-power X3 frequency multiplier
- Produced a flexible and upgradable digital phase-lock loop
- Achieved low projected reproduction cost as a result of leveraging off high-technology commercial developments

### Table 1. Receiver performance goals.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Near Earth</th>
<th>Deep Space</th>
</tr>
</thead>
<tbody>
<tr>
<td>Center frequency</td>
<td>2025–2110 MHz (S band)</td>
<td>7145–7190 MHz (X band)</td>
</tr>
<tr>
<td></td>
<td>7190–7235 MHz (X band)</td>
<td></td>
</tr>
<tr>
<td>Noise figure</td>
<td>≤2 dB</td>
<td>≤2 dB</td>
</tr>
<tr>
<td>Carrier acquisition threshold</td>
<td>–130 dBM</td>
<td>–158 dBM</td>
</tr>
<tr>
<td>Two-sided carrier loop bandwidth</td>
<td>800 Hz (no limiter)</td>
<td>18 Hz (with limiter)</td>
</tr>
<tr>
<td>Acquisition sweep rate</td>
<td>≥35 kHz/s @ $P_c = -100$ dBm</td>
<td>≥400 Hz/s @ $P_c = -110$ dBm</td>
</tr>
<tr>
<td>Carrier tracking range</td>
<td>≥250 kHz from center frequency</td>
<td>≥250 kHz from center frequency</td>
</tr>
<tr>
<td>Radiation tolerance</td>
<td>~25 krad (greater with shielding)</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>&lt;1.5 W @ 5 V (standby); &lt;2.5W @ 5 V (operational)</td>
<td></td>
</tr>
<tr>
<td>Size</td>
<td>4 x 4 x 0.75 inches (10.2 x 10.2 x 1.9 cm)</td>
<td></td>
</tr>
</tbody>
</table>

### Table 2. Breadboard X-band receiver power consumption as a function of subsystem.

<table>
<thead>
<tr>
<th>Subsystem</th>
<th>Volts (V)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low noise amplifier</td>
<td>5</td>
<td>274</td>
</tr>
<tr>
<td>Down-converter</td>
<td>3.3</td>
<td>304</td>
</tr>
<tr>
<td>Digital phase-lock loop</td>
<td>5</td>
<td>212</td>
</tr>
<tr>
<td>Frequency synthesizer</td>
<td>3.3</td>
<td>130</td>
</tr>
<tr>
<td>X3 multiplier with amplifier</td>
<td>3.3</td>
<td>294</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>1214</td>
</tr>
</tbody>
</table>
Performance excellence and high reliability are and historically have been the primary goals for APL ultrastable quartz oscillators (USOs). APL oscillators have demonstrated Allan variance frequency stability of $<5 \times 10^{-14}$ (10 s) and aging rates of $<7 \times 10^{-13}$/day. The quartz resonator is the heart of a USO and dominates its frequency stability. The electrical, thermal, and mechanical features of a USO design have one goal—to establish the optimum stable conditions for resonator operation. The primary obstacle to consistent production of space-qualified oscillators with $<5 \times 10^{-14}$ frequency stability is the quartz resonator, because very few quartz resonators (on the order of 1%) have $<5 \times 10^{-14}$ frequency stability.

The only successful method we have found to identify superior performing resonators is to conduct screening tests on each resonator. Large quantities (10 to 20 times the number needed) of resonators are purchased at a cost of up to $3000 each. Each resonator is installed into a test oscillator with known performance and screened for Allan variance, aging rate, phase noise, sudden frequency changes, and radiation sensitivity. Resonators often meet two or three of the parameters but fail the others. Screening is an expensive, time-consuming process that has a low yield of acceptable resonators. This, coupled with the cost of purchased resonators, can cause the real cost of flight-qualified resonators to exceed $50,000 each in a worst-case scenario.

The simple availability of high-precision quartz resonators is a problem of equal magnitude. Over the past few years a series of events has reduced the potential vendors of high-precision quartz resonators from three to ZERO. Without a reliable source of high-precision quartz resonators the capability to produce USOs does not exist.

This ATD development task was initiated to develop a new reliable source of high-precision 5-mHz quartz resonators. The objective of this project is to develop a quartz resonator with an Allan variance of less than $1 \times 10^{-13}$ (10 s) that has no sudden frequency changes greater than $1 \times 10^{-12}$ and that can be manufactured with consistent performance from unit to unit. The resonator development is focused on two major tasks: (1) a metallic brazing process to join the quartz resonator plate to the mounting support ribbons, and (2) optimization of the quartz resonator plate design. A third task, an in-depth study to determine the technical and economical feasibility of developing a reduced height, or low profile package (LPP), for the resonator enclosure, has been completed with the conclusion that the LPP is feasible. A report was published presenting the results. This new LPP resonator would enable a smaller USO to be developed that can be reliably produced with frequency stability $<1 \times 10^{-13}$ (10 s), mass $<350$ g, volume $<300$ cm$^3$, and input power $<0.6$ W. The resonator development is a collaborative venture between APL and Piezo Crystal Company.

Most quartz resonators are fabricated with conductive cement to attach the quartz resonator plate to the mounting support ribbons. The joint between the resonator plates and the support ribbons is a critical mechanical, and a very sensitive electrical, connection. It is extremely difficult to maintain a process control that will consistently produce acceptable joints. The conduction path through the cement is poorly defined, not well understood, and does not produce consistent low-resistance joints. Because the oscillator...
frequency sensitivity to impedance change is \(1 \times 10^{-12}/\text{ohm}\), fractional resistance changes in the conduction path produce unacceptable frequency changes. Variations in the Allan variance of 10 to 1000 within a lot of identically processed cemented resonators are common. Sudden frequency changes as large as \(1 \times 10^{-10}\) with random duration and spacing in time are also common. Extensive data accumulated at APL clearly show that quartz resonators fabricated using a gold germanium brazing process to attach the quartz resonator plate to the ribbon support mounts have superior frequency stability with few sudden frequency changes.

The goal to design a frequency stability of \(<1 \times 10^{-13}\) (10 s) into the resonator that can be produced consistently is ambitious and has not previously been achieved. With the current resonator and raw quartz technology, the probability of improving resonator frequency stability performance by more than 10 is unlikely. By optimizing the resonator design and implementing the LPP, an improvement in frequency stability by a factor of approximately 5 has a high probability of success.

The choice of resonator design variables is large and will produce resonators with a wide spread in the motional parameters \(L_1\), \(C_1\), \(R_1\), and \(Q\). The shape, or diopter, of one resonator surface is a parameter we have chosen to investigate. Resonators with a diopter variation between 1 and 7 have been designed and verified by fabricating resonators using cemented technology. The resonator diopter also has a dramatic effect on the resonator frequency’s sensitivity to changes in drive level, or the current passing through the resonator. A small diopter has a lower drive level sensitivity. The literature suggests that the best frequency stability is achieved with a large \(L_1\) and a low drive level sensitivity. Our experience has shown that smaller values of \(R_1\) and the accompanying low drive level sensitivity yield the best frequency stability. As discussed earlier, these requirements are in direct conflict as a function of resonator diopter. A partial set of these designs will be repeated with brazed resonators to determine the optimum resonator plate design.

The process to braze and finish quartz resonators is complex and tedious, and requires careful attention to small but important details. The brazing process developed by Piezo produces very good melting and flow of the brazing material between the resonator plate and the mounting support ribbons with consistent results and a 90% success rate. Visual appearance of the brazed joints is very good, and during bond pull tests the brazed interface broke at 1.8 pounds. The relative merit of this number is not easy to comprehend. However, when the brazed joint broke, quartz was pulled from the resonator plate and remained attached to the mounting ribbon. The bottom line is that the brazed joint is stronger than the quartz.

We have been successful in producing the critically important brazed joints; however, other parts of the overall fabrication procedure remain to be resolved. The sequence of new added metal disposition required in the brazing process and the physical handling of the resonator plates during fabrication to maintain pristine cleanliness requires additional work. None of these processing steps are insurmountable; the details simply need to be addressed.

The \(Q\), or quality factor, is the best measure of potential resonator performance. The \(Q\) of the brazed resonators is much higher than normal. One resonator had a \(Q\) of 3.09 million; another had a \(Q\) of 3.19 million. The \(Q\) values are 96% and 99%, respectively, of the maximum theoretical values that can be achieved. These are the highest \(Q\) values either Piezo or APL has ever observed for a 5-MHz resonator. (The average \(Q\) for cemented resonators is 2.3 million.)

The best Allan variance for the small number of brazed resonators tested is \(3.5 \times 10^{-13}\), well short of our design goal. The most likely cause of this poor performance is the incomplete fabrication process, particularly the very critical task of minimizing contamination of all the resonator parts during fabrication and assembly.

Funding has been received from an independent source to continue with the resonator development initiated by this task, including development the LPP resonator package.
Advanced Architectures

The ATD program’s advanced architectures thrust area is exploring technologies for revolutionary data communications, computing, power, and propulsion techniques that may fundamentally change the nature of space missions. The technologies that we are exploring will bring significant reductions in individual spacecraft mass and cost, large gains in capabilities and robustness, and novel architectures suitable for large constellations and closely coupled spacecraft.

1394 Serial Bus Development

The ATD program is improving the use of the IEEE 1394 serial bus for subsystem communications on spacecraft. IEEE 1394 is well suited for this purpose because its protocols are robust and rigorously defined, throughput is large but power consumption is modest, and redundant configurations are feasible when needed to support missions of long duration. We are also assessing the survivability of several interconnect topologies. Spacecraft system designers can use these results to balance redundancy and cost against mission requirements. We are particularly concentrating on algorithms which permit communication between multiple IEEE 1394 buses within a spacecraft. Using several buses on the spacecraft increases available bandwidth, increases isolation between subsystems, and eases development. The ATD program’s goal is to investigate the feasibility of developing a bus interface that integrates these functions onto a single chip.

Power Systems Architecture

Both the commercial and government sectors have made a significant investment in the development of ultra-low power digital (ULP) electronics. Government investment has been focused on the combination of ULP (with power reductions of 2 orders of magnitude over existing systems) with radiation hardening specifically needed for spacecraft applications, an area with limited commercial potential. This radiation-tolerant ULP technology will be realized in 1–3 years. Spacecraft design could be significantly affected by ULP electronics. As a result, the ATD program is beginning to answer the question: “What major changes in spacecraft design could ULP technology enable in the next 5 years?”

Martin Fraeman

Current spacecraft designs include the following subsystems: structure, thermal control, power generation and distribution, external communications, internal communications and control, and guidance and control. Specific functional requirements are mission dependent, but new technologies like ULP enable practical solutions to be found for current and future problems. ULP electronics will both directly and indirectly affect spacecraft design. The most obvious direct impact of ULP is that the power necessary for electronic circuits will be greatly reduced. Indirect benefits from ULP insertion on power generation and distribution, thermal management, attitude control, and overall spacecraft bus design and organization may be even more significant. How ULP electronics are applied will determine the savings that can be realized in power, mass, and complexity in overall spacecraft design. ULP technology may also enable entirely new types of spacecraft (e.g., nanosats the size and mass of a soda can) and missions (e.g., swarms of nanosats).
**Spacecraft Quantum Computing**

NASA has recognized the revolutionary potential of quantum computers and other forms of quantum information processing. Quantum computers are expected to be able to solve numerical problems that would not be feasible to solve on conventional computers, and the ATD program has focused on this critical area. Roughly speaking, a quantum computer can perform a large number of calculations simultaneously on a single processor using nonclassical logic operations.

The goal of achieving a quantum computer in space is very long range. The immediate goal of the ATD program was to demonstrate an efficient XOR quantum logic gate based on an optical approach that APL has been pursuing for several years. APL and the Jet Propulsion Laboratory (JPL) are collaborating on a more detailed theoretical analysis of the basic physical mechanism and on ways to improve the performance of the quantum logic gates. JPL’s expertise in quantum logic circuits could be used to design simple circuits for eventual implementation and testing using APL-developed hardware. Some of these ATD program techniques may also be useful in producing the necessary input states for a high-precision quantum gyroscope that JPL is investigating.

**Advanced Systems for Chemical Propulsion**

Spacecraft are shrinking, and propulsion system components must shrink along with electronics. The ATD program is developing key technologies for propulsion subsystems for small satellites.

A miniaturized pressure transducer, with mass and power consumption an order of magnitude lower than that of current transducers, combined with integrated signal processing electronics is being developed. The flow-through sensor is contained in a low-mass inline housing. Local conditioning electronics, eventually based on APL’s radiation-hard, mixed-signal, low-power, analog-to-digital converter (the TRIO chip) technology, will digitize sensor output. The electronics will be compatible with a distributed engineering data collection methodology so that the mission-specific configuration of pressure transducers configuration does not affect the main spacecraft electronics design.

The ATD program is also developing a miniaturized, lightweight integrated tank/thruster assembly. We gained initial experience by building an integrated cold gas storage and thruster assembly using conventional manufacturing technology to save development cost. Eventually, chemical machining should be used to build an even lighter cold gas propulsion system with integrated valve and thruster assembly. Such a tank/thruster assembly saves mass and is well suited to very small satellite applications. This kind of assembly can also be mounted directly to a printed circuit board containing support electronics and is well suited to distributed control. As with the pressure transducer, that architecture removes mission dependencies from main spacecraft electronics design, encourages reuse, and, hence, reduces cost.
The IEEE 1394 High Performance Serial Bus Backplane Profile defines both hardware and software conventions for communicating high-throughput information between subsystems onboard a spacecraft. The 1394 Serial Bus ATD program concentrated on improved backplane profile design, interconnect policies, and topology survivability analysis.

An APL Independent Research and Development project has designed a dual-channel, fault-tolerant, IEEE 1394 Backplane Profile Bus Interface Unit (BIU). The design supports asynchronous block data transfers over a primary channel with provisions to use a secondary channel in case the primary is blocked. As this design has matured we have identified several improvements that would enhance its use within spacecraft. These include a method to extend the backplane profile across a small number of electrically isolated segments; a programmable link/physical layer clock ratio to enable much higher speed transaction rates; and more extensive support of bus monitoring/stimulation to improve on-board bus safing and ease system integration testing.

The ATD program has implemented these improvements. The existing VHDL hardware description language-based BIU design has been modified, and a field programmable gate array (FPGA) breadboard prototype was built to verify correct system-level operation. The test bed incorporates four bus nodes. Host processors control two nodes. The other two nodes transfer data directly between the local address space and the bus without any external computer support. The FPGA implementation of the dual-channel BIU design fits into less than 300,000 gates and 80 kbits of memory, well within current radiation-hard application-specific integrated circuit fabrication capabilities.

IEEE 1394 permits a single bus to have up to 63 nodes. The standard also includes protocol fields that support up to 1023 buses, meaning that a theoretical maximum of up to 64,449 nodes can be addressed. Multiple node address regions could provide important benefits. For example, overall maximum data transfer bandwidth available on the satellite would be improved, and it would be possible to isolate traffic local to a specific task. A hierarchical bus structure based on the use of the same data transfer mechanisms both within and external to subsystems would also improve technology reuse.

The ATD program has investigated algorithms needed to support data transfers between multiple IEEE 1394 buses. Solutions to a variety of issues are being studied with the goal of showing how a bus bridge to connect independent local buses can be built. The bridge will forward non-local packets and generate acknowledge packets to the local sending node. The bridge will also detect a remote transaction failure and send an appropriate response packet back to the originating local node. External traffic with a local node destination must also be properly handled. Local destination failure as well as success must generate an appropriate response to the originating external node, perhaps through multiple intervening bridge nodes. The complexity of solutions to these issues means that a purely hardware-based IEEE 1394 bridge is not currently practical. Instead, a true bridge requires processor control of interface chips such as our BIU.
The topology of node interconnections affects system survivability since problems with individual components occur in space missions of long duration. Probability of mission success is enhanced by robust connectivity between primary and secondary resources. At one extreme, a topology that consists of two independent sets of electronics can survive a single failure by replacing the primary resource with its backup. A failure anywhere in the now activated backup unit will end the mission. A far more robust approach would be to break the design into several subsystems with extensive cross-strapped connections between primary and secondary subsystems. A single fault in a subsystem is remedied by activating its backup unit. Additional faults are tolerated as long as they do not occur in a backup subsystem that is already in use.

Comparing proposed interconnect topologies that balance implementation costs against robustness is challenging. Traditionally, probabilities of failure are assigned to each component of a proposed design and then the overall probability of mission success is computed. Small differences in initial estimate of module failure probability strongly affect the final calculation and can easily change the apparent best interconnection choice. Furthermore, module failure rates cannot be accurately estimated. Components used are generally so reliable that an insufficient number of devices have been manufactured and operated long enough to gather accurate lifetime statistics. The problem is exacerbated for space-based applications because so few operating hours in that environment have been accumulated, especially for new state-of-the-art components needed to implement the challenging missions of the future.

The ATD program has developed an analysis technique that compares the fault tolerance of different proposed topologies independent of any initial (and of necessity, inaccurate) estimate of component reliability. A network design can be selected on the basis of its merit without making assumptions about the connected nodes. The analysis technique was initially developed to study data network topologies for the U.S. Navy to improve ship survivability under battle conditions. The ATD program has applied this technique to compare several satellite subsystem interconnect topologies. Specific connections that were studied include an example of current satellite design practice (the TIMED spacecraft) and, the IEEE 1394 Backplane Profile based APL integrated electronics Module. The MESSENGER spacecraft is now using the technique to investigate alternative electronic architectures.
One of the scarcest resources on board any spacecraft is energy. We want our space systems to do more for less, but providing more energy to a spacecraft necessarily implies increased cost—especially increased launch cost. This raises the questions: Could we do more for less power? Does greater functionality necessarily imply greater energy demand?

All modern space missions use digital microelectronics for guidance, navigation and control computing, instrument and sensor data processing, and command and data handling. An ultra-low-power (ULP) digital electronics technology is being developed by a team led by the University of New Mexico NASA Institute of Advanced Microelectronics (UNM IAµE) that uses 1 to 2 orders of magnitude less power than conventional integrated circuits while retaining comparable performance.

ULP technology builds high-performance active digital circuits with greatly reduced power consumption. ULP operates with supply voltages of 0.5 V or less. The CULPRiT (CMOS Ultra Low Power Radiation Tolerant) technology program led by the UNM IAµE combines ULP with radiation mitigation techniques. ULP devices are manufactured using standard commercial semiconductor fabrication processes and have operating characteristics similar to those of standard complementary metal-oxide semiconductor (CMOS) devices. CULPRiT uses standard design and development tools and is screened and packaged like other CMOS integrated circuits—all without exotic techniques or materials. ULP capability requires minor changes to the fabrication process parameters, together with special circuit techniques for biasing and controlling ULP devices.

The CULPRiT team is developing a 0.35-µm CMOS ULP technology at a major commercial foundry. Three ULP foundry runs have been completed. The first included transistor array test circuits, and the next two consisted of multi-project runs. ULP chips that have been built include radiation test chips, transistor arrays for model extraction, and full-function special-purpose processors such as telemetry channel coders. A radiation-tolerant ULP Reed-Solomon encoder chip consumes 330 times less power than the most commonly used equivalent flight component while operating at an identical throughput rate. Total dose radiation tolerance of ULP chips has been tested well in excess of 100 krad, and the cell library includes functions designed using radiation-induced single event upset (SEU) immune circuit techniques.

APL, in conjunction with some of the CULPRiT team members, has determined that 20–40% of the power used by a spacecraft can be saved by extensive use of ULP digital electronics. The greatest percentage power reductions will be for relatively small, moderate-bandwidth spacecraft.
with passive sensors. A relatively modest percentage reduction will translate into a healthy improvement in mass margin for a particular mission or increased power available for other functions. Reducing a spacecraft’s load power has other immediate first-order benefits to life-cycle cost: the power subsystem becomes smaller, lighter, and cheaper, and there is less heat to remove from the electronics. There are also potentially important second-order effects, which are more difficult to quantify. For example, a smaller solar array enables smaller attitude control actuators to be selected. For space missions that require propulsion, the reduced battery and solar array mass would, in turn, require less propellant, so that for spacecraft in high ΔV cost orbits (e.g., geosynchronous orbit), the benefit is amplified by an appreciable factor.

One of the ATD program’s key efforts is to determine alternative approaches to generating, conditioning, and distributing power to ULP-based subsystems. We have also sought to identify other technologies needed to achieve the potential benefits of ULP technology on spacecraft. A spacecraft subsystem built entirely with ULP digital electronics will have very different power supply needs than a subsystem with equivalent current digital designs. Obviously much less power will be needed, and a distributed power architecture is attractive. ULP technology will use very low power supplies (≤0.5 V) with an associated reduction in signal amplitude. Hence noise margins are lower than traditional logic families. Electromagnetic interference and compatibility of ULP circuits are not known but are of concern since signal amplitudes are so low. Potential noise sources may include cross talk between ULP and non-ULP signals, power supply coupling of noise between ULP chips, and on-chip bias generator circuits. Hence a power source that can deliver up to 0.5 A at sub-volt levels is needed. High efficiency must be achieved or more power will be consumed in the supply than in the actual ULP application circuit. The source must also provide sufficient regulation and noise rejection to ensure proper operation of a ULP-based subsystem.

The ATD program evaluated potential ULP power supply design architectures. We focused our development on a converter that will use a 3.3-V or 5-V input source and produce a regulated 0.5-V output for a nominal 0.5-A load. This capacity converter should be well matched to a board design that makes extensive use of ULP technology. We developed a schematic design for the power path electronics (input and output filters, field effect transistor [FET] power switches, dead band control, gate drive electronics) of a buck switching regulator for ULP applications.

A prototype unit of the ULP buck switching regulator was designed and tested. The unit was powered from a 3.3-V laboratory power supply and delivered 0.5-V into a 0.25-W load. The breadboard was used to determine the timing relationship between power FET switching events. That information was used to establish performance expectations for ULP power supplies and to determine feasible requirements for a more integrated converter design. The feedback control circuitry that compares the output voltage to a fixed reference and sets the regulator duty cycle was not included in the initial design. This function was simulated with an external oscillator that provided regulator pulse width control into a high-impedance input. The regulator was tested at a nominal switching frequency of 50 kHz although operation up to 100 kHz was verified. The ULP regulator operated as designed with a measured power efficiency of 75%. A simple improvement to the prototype unit (eliminating unused low-power voltage comparator elements) should improve the efficiency by a few percent.

The ULP converter was integrated with a ULP-based Reed-Solomon encoder being developed at the NASA Goddard Space Flight Center. In order to ensure compatibility of the two designs, the regulator output voltage was adjusted to 0.6 V. In addition, a second low-pass filter stage was added to reduce conducted output voltage ripple. The Reed-Solomon encoder functioned properly when powered by the ULP converter prototype. The converter operated at a slightly higher efficiency at the higher output voltage.

http://sd-www.jhuapl.edu/ATD_NASAAPL/
Quantum computers have the potential to perform numerical calculations that would not be feasible on conventional computers. Roughly speaking, quantum computers can perform many calculations simultaneously on a single processor (quantum parallelism), which is expected to exponentially increase the effective speed of the calculations. In addition, quantum computers can use quantum logic operations to perform calculations in a way that has no classical analogy.

NASA has recognized the revolutionary potential of quantum computers and other forms of information processing, and a rapidly growing group of researchers in this area is active at the Jet Propulsion Laboratory (JPL). Potential NASA applications for quantum computing include autonomous decision making by distant probes and on-board data analysis and compression in order to reduce the volume of data to be transmitted by remote spacecraft. This ATD project has supported a collaboration between JPL and APL over the past 2 years. The basic goals of the project were to perform a more thorough theoretical and experimental analysis of APL’s optical approach for building the basic quantum logic gates required for quantum computation. Additional goals included the design of simple quantum circuits using these devices and collaborative efforts in related areas, such as quantum gyroscopes.

APL is investigating an optical approach to quantum computing in which the quantum bits of information (qubits) are represented by single particles of light, or photons. The primary advantage of this approach is that photons can be transmitted over relatively large distances using optical fibers or wave guides, which allows arbitrary connections to be made between the various logic and memory devices, as is the case for conventional computers. In contrast, most alternative methods for quantum computing rely on nearest-neighbor interactions and would not permit the use of a conventional bus architecture, for example. Additional advantages include high speed, low sensitivity to the environment, and a simple structure that may allow the fabrication of large numbers of devices on a single substrate.

Logic operations using single photons require that one photon be able to control the state of a second photon, which corresponds to a nonlinear process at very low intensities. In conventional mechanisms for nonlinear optics, two photons are required to interact with the same atom in a medium containing a large number of atoms. Here the absorption of photon 1 by an atom will change the state of the atom, which in turn changes the effects of that atom on a second photon. Unfortunately, the probability that two photons will interact with the same atom in an ordinary medium is very low; thus these kinds of interaction are usually negligible. In our approach, two photons interact with two different atoms. Atom A absorbs photon 1 and re-emits photon 2, while atom B absorbs photon 2 and re-emits photon 1. This exchange of photons produces a nonlinear phase shift that can be used to implement quantum logic operations. Effects of this kind are relatively large since the photons can interact with any atoms in the medium and are not required to interact with the same atom.

Our earlier theoretical analysis of the operation of these devices was based on a number of
approximations, including the assumptions that the medium was very thin, that the coupling of the photons and atoms was weak, and that the atoms were stationary. More detailed calculations were performed in collaboration with JPL in order to eliminate these assumptions and obtain more realistic results. The theory was generalized to include the case of a thick medium by describing the excited atoms as a quantum superposition of excited states (Dicke states). The application of short laser pulses to the medium while the photons are inside was also analyzed and found to allow efficient logic operations to be performed in a short time interval. The potential advantages of using an inverted medium were also considered, and the design of suitable sequences of laser pulses was formulated using the commutation properties of quantum-mechanical operators.

The experimental apparatus we used to investigate effects of this kind was improved in a number of ways. The atoms required for the interaction to take place are generated by heating sodium in a vacuum cell. New sodium cells were fabricated using stainless steel chambers and sapphire windows, which extended the useful lifetime of the cells from a few days to many years. We developed a method for compensating for the birefringence in the cell windows. We substantially improved the signal-to-noise ratio and the stability of the experimental results by adding computer-controlled piezo-electric elements to automatically align the optics. We added two computers to the system to control the optical components and to increase the data collection rate.

Some typical experimental results are shown. Roughly speaking, the experiment is designed to send two photons through an atomic medium (sodium vapor), either at the same time or at two different times. The predicted nonlinear interactions between the two photons are expected to increase the probability of detecting both photons only if they pass through the cell at the same time. The peak in the center of the figure shows that the detection probability is higher when the photons pass through the cell at the same time, as would be expected from the theory. Although this result is encouraging, the nonlinear phase shift that was obtained was too small to allow the construction of working logic gates. A modified experiment using a sequence of laser pulses is expected to produce a nonlinear phase shift of π, which would allow the construction of logic gates and simple quantum circuits.

JPL and APL also collaborated in several other areas, including a discussion of various approaches to quantum gyroscopes. A joint paper describing a new form of geometrical (quantum) phase was published in Physical Review Letters; a second paper has been submitted to Physical Review A.

Some preliminary experimental results, which show the rate of coincident photon detection as a function of the difference in the arrival times of the two photons at the detectors. The peak at zero delay time in the center of the plot provides evidence for the expected interaction of two photons when they pass through the medium at the same time.
In order to provide low-mass and low-power options for small-satellite (20–100 kg) propulsion and attitude control, the Advanced Technology Development (ATD) program has developed an integrated miniature nitrogen cold gas propulsion system and a lightweight pressure transducer with an I²C digital interface. Small-satellite mission and system requirements have a broad range, depending on the details of the specific mission. The miniaturized pressure transducer and cold gas propulsion system are aimed at missions with low mass, low power, and total impulse requirements and a thrust level that could vary from 0.1 N to 5.0 N. The final thrust level would depend on whether attitude control precision or the time available to impart a given delta V dominates the impulse requirements.

The ATD program developed a miniature cold gas propulsion system architecture specifically designed to meet the requirements of low-mass and low-power small-satellite applications. After a small spacecraft or constellation is launched and after the tip-off rates induced by separation are corrected, the onboard propulsion system provides impulse to place the spacecraft into the final orbit or appropriate position within a constellation. Thereafter, further constellation position correction would be provided. The miniaturized cold gas propulsion system could also be used for momentum dumping of a reaction wheel control system or for precision attitude control.

The ATD program’s low-mass cold gas propulsion system (built and tested by VACCO) uses only four double canted thrusters to achieve the required three-axis control during and after the required delta V maneuvers. The design uses latching solenoid valves to save power. With standard solenoid valves, the power must be engaged at all times to maintain the position of the solenoid, while the latching solenoid approach uses significantly less power since the solenoid is powered on for only <50 ms when changing the position of the valve poppet.

We did not know whether the newly designed latching solenoid would be responsive enough because of the response time needed to open and then close the latch. A typical nonlatching solenoid valve can provide a very short impulse bit to finely control the system. The smaller the impulse bit, the finer the pointing control achieved. Although highly accurate pointing or attitude control is not typically implemented with thrusters, the function may be desirable as a high rate backup or for momentum dumping. Final acceptance testing of the ATD system at VACCO showed that impulse bit timing as low as 10 ms equivalent on time is possible with the latch valve approach. Latch valve open/close response times less than 8 ms were demonstrated over the blow-down range of 3500–25 psia.

Some cold gas systems require regulators to reduce the storage pressure to a constant operating pressure. In the ATD design, we further reduced mass by eliminating regulators so we can operate directly from storage pressure in a blow-down mode. This was made easier by using latch valves instead of solenoid valves because they can be designed to operate against a higher delta pressure across the valve seat while maintaining low total power. Latch valves can also generate higher seating forces at the poppet, which can result in significantly less potential for leakage.

The next step in further integrating the cold gas system would be to adapt VACCO’s CHEMS™ technology for manufacturing various propulsion system control and distribution elements. VACCO’s CHEMS™ technology can use chemical machining techniques to build miniature, lightweight propulsion assemblies for small satellites. Key components include chemically machined and diffusion bonded manifolds, regulators, filters, valves, and thruster nozzles using several layers of etched elements.

Present propulsion system pressure transducers draw 1 W of power, weigh 0.2–0.5 kg, require mounting, and have individual harnesses back to...
the command and data handling and power subsystems. It is possible to develop a low-power (<0.1 W) miniature sensing element and install it in an in-line housing with adjacent or integrated signal conditioning and digitization circuits. A low-speed, low-power utility bus can be used to digitally connect multiple addressable devices to the rest of the spacecraft electronics.

The ATD program contracted with GP:50 Aerospace to develop a transducer with the described attributes. GP:50 was uniquely qualified and possessed the exclusive manufacturing license for all development and manufacturing from NASA Marshall Space Flight Center for the miniaturized silicon technology microsensor required for the pressure transducer. The ATD program has designed, built, and tested the following:

- Three miniature high-pressure flow-through transducers using a silicon sensor substrate mounted protected from corrosive medium by a high-pressure passive diaphragm and header: one 0–500 psia, 55-g unit with integrated electronics; one 0–5000 psia, 55-g unit with integrated electronics; and one nondelivered 0–500 psia, 10-g unit with separate electronics.
- A PC board for power regulation, digital communication, and interface manipulation that interfaces with the sensors via four wires and feeds a 10-bit address standard I2C protocol.

We achieved significant advances in mass and power efficiency. Our performance goals were a transducer with a mass of less than 55 g and power consumption of less than 0.1 W. Minimum harness mass per foot, based on the number of wires and wire gauge, was a secondary goal. Sensor electronics were based on a commercially available low-power microprocessor with an integrated analog-to-digital converter and I2C interface. The electronics also included a power supply regulator, an amplifier, and a temperature-sensing transducer. All these electronics could be integrated into a single chip using the design techniques developed for APL’s radiation-hard TRIO and microDSAD chips.

A radiation exposure test of a GP:50 Model 7100 transducer (a model that contains the same sensor and temperature compensation electronics as the test transducers) was also completed. The test was stopped at 116 krad (after about 2 days of testing), and the transducer was still functional. An overall zero shift of about 1% was observed during the test. The shift was proportional to dose. Recalibration of the transducer at GP:50 showed no change in the slope of the calibration curve after the radiation exposure.

Units using some or all of the digital interface and miniature elements of the ATD program units are baselined or being considered for use on NASA Marshall’s Shuttle Upgrade program, the Jet Propulsion Laboratory’s Europa Orbiter and X2000 programs, and NASA Goddard Space Flight Center’s ST-5 Miniature Propulsion program. From the results of the radiation testing under the ATD program, the Jet Propulsion Laboratory has expressed interest in further radiation testing of the transducer-sensing element for the Europa Orbiter.
Spacecraft in Earth orbit provide communications, reconnaissance, and scientific analyses on a global scale. Beyond Earth orbit, robotic space probes explore our solar system, returning images and data that answer our questions and invariably create new puzzles. One-way, sample-return, and, eventually, piloted missions promise to deepen our awareness of our true home: the solar system.

Spacecraft all share the common purpose of delivering our carefully constructed measurement technology: the instruments. Ultimately, the success of a mission depends on the ability of instruments to make the measurements that drove the mission’s creation. Because of the stringent requirements on spacecraft instrument reliability, fault tolerance, mass, and power consumption, instrument design and fabrication has developed into a specialized field of expertise. Instrument development has required extensive rethinking of original techniques. Nowadays, the ambitious goals for space missions, particularly in situ planetary probes, require even more extensive development of the technologies that both enable instruments to function and enable the synergy of instruments with their supporting spacecraft.

The Instrument-Enabling Technologies thrust of the ATD program has concentrated on six technologies of key importance for the coming era of ultra-miniature, ultra-capable spacecraft instruments. These technologies take advantage of new materials and methods, new physical phenomena, and new commercial drivers to enable instruments using optical filters, mechanical components, thermal control, tunable lasers, sample handling and vacuum systems, and particle detection.

**Mechanical Methods for Instruments**

Micro-satellites, precision instrument deployment, and in situ manipulation systems for increasingly sophisticated missions call for development of highly miniaturized and rugged mechanisms. Although off-the-shelf mechanical components for small satellites are relatively compact compared to those in many Earth-bound devices, for the most part they do not approach the ultra-miniature size required for sub-meter-scale spacecraft and centimeter-to-millimeter scale instrumentation. New materials, fabrication processes, and geometries must be considered for these critical components to operate reliably and reproducibly.

The ATD program, in collaboration with Starsys Research, Inc., is developing truly miniaturized off-the-shelf micro-mechanisms. This micro tool kit includes six new mechanisms: the Mini Separation Nut, the Micro Separation Nut, the Mini Rotary Actuator, the Mini Burn Wire, the Mini Linear Actuator, and the Mini Redundant Release Mechanism. All are on the sub-centimeter scale and were produced in iterations with careful consideration of the scaling of performance, tolerances, and power requirements. Five of the devices are new implementations of shape memory alloy materials, which deform reproducibly with a change in temperature. The mechanisms were extensively tested and show great promise to enable deployment and manipulation in a broad range of instrumentation.

**Thermal Methods for Instruments**

Significant reductions in instrument and spacecraft size, mass, and power levels are possible with new materials and techniques, but novel control systems are needed that permit the instruments to operate in the harsh environment of space. Paramount among these systems is the retention, transfer, and dissipation of heat, especially where small instruments must survive extreme thermal cycling and must operate in cryogenic conditions. While conventional direct, controlled heating and radiative cooling has been quite successful in past missions, thermal control systems have to be re-thought for use on the ultra-small-scale space probes of the future. In partnership with Starsys Research, Inc. and Virginia Tech, APL has worked toward a thermal control model.
that relies on internal instrument power. A novel thermal switch, a high-conductivity composite radiator, and a tailorable control surface are included in the Miniature Spacecraft Energy Retention (MISER) panel, which would particularly enable long-transit planetary missions and “micro-sat” type constellations.

**Resonant Laser Methods for Instruments**

Sensitive composition measurements at a fine spatial scale are increasingly important in landed science missions, for *in situ* studies as well as sample-return reconnaissance. Elemental, isotopic, molecular, and mineralogical micro-analyses all provide information for placing a sample in geochemical context. These analyses must be able to detect the presence of specific species at low levels and within heterogeneous samples.

The Resonant Laser Methods ATD project is a step toward achieving this goal with techniques that can enable miniature mass spectrometers, fluorescence spectrometers, and other composition instruments. New, compact optical parametric oscillator (OPO) laser technology has been incorporated into a set of optical focusing systems. The OPO permits a wide range of wavelength tuning without sacrificing the laser energy, power draw, mass, or ruggedness advantages of composition sensors under development. Several optical coupling geometries and measurement algorithms were tested to determine the feasibility of using OPO technology in a miniature *in situ* probe. We found that careful control of the focusing optics and particle detector inlet geometry can enable resonant enhancements. The technique shows significant promise for detecting minor elements that would otherwise be lost in the noise of major components and for characterizing important stable organics such as polycyclic aromatic hydrocarbons.

**Sample Handling and Vacuum Systems for Landed Instruments**

Some of the highest performance analytical techniques, such as electron microscopy, mass spectrometry, and x-ray diffractometry, are challenging to implement on space probes because they require precise sample preparation, sample manipulation, and high-vacuum conditions. The great benefits obtainable from miniaturized, automated versions of these methods are strong drivers for developing *in situ* sample and vacuum system (SVS) technology. In particular, careful microanalyses of solid samples, available only from such instruments, can provide critical data for sample-return selection as well as for long-duration science surveys.

The SVS project has focused on enabling the acquisition, vacuum insertion, manipulation, and positioning of small solid samples. A partnership with Creare, Inc. has furthered the development of ultra-miniaturized, low-power turbomolecular pumps (TMPs) for remote operation, by both testing an initial TMP prototype under realistic instrument conditions and designing an enhanced TMP for operation on Mars with no backing pump. All SVS components are significantly smaller and lighter than the high-capability instruments they enable, providing the potential for a high level of *in situ* capabilities.

**Compact Hyperspectral Imagers**

Development of compact, rugged optical filter technology will enable substantial reductions in the complexity of spacecraft imagers and an increase in their reliability. A major step in this development is the replacement of mechanical filter selection by intrinsically wavelength-tunable filter components. The ATD program has studied electronically variable liquid crystal tunable filters (LCTFs) for use in spacecraft hyperspectral imagers. LCTFs can provide a swift, motionless selection of wavelength for multi-spectral, high-resolution images using monochrome charge coupled device cameras. A vital issue for using such advanced materials in space is their response to radiation. The effect of total dose on LCTF transmission and on the LCTF components was studied over the full visible wavelength range. After being radiated up to 71 krad, the LCTF suffered transmission losses of a few to several percent, depending on wavelength, with a saturation trend.

**Flat Plasma Spectrometer**

Constellations of tiny spacecraft (the micro/nano/pico-sats) are part of the long-term plan to comprehensively study the heterogeneity and dynamics of the space environment. Detailed, simultaneous, multi-point analyses of magnetospheres will require new miniaturized plasma spectrometers with a high ion throughput-to-volume ratio. The Flat Plasma Spectrometer (FlaPS) technology development effort has investigated the possibility of fabricating extremely compact and low-power charged-particle instruments with microelectromechanical techniques. FlaPS approaches angular coverage with a surface tiling model rather than a traditional rotating, bolt-on instrument. A collaboration with NASA/Goddard Space Flight Center and The College of William and Mary has produced a centimeter-scale instrument prototype.
With the current push for micro-satellites in the range of 10–100 kg comes a new era in mechanism design. Advances in the variety and processing of materials have created abundant opportunities to miniaturize mechanisms. While many off-the-shelf mechanisms are very compact, they are not the order of magnitude reduction in size needed for micro-satellites. This ATD project focuses on the design and development of six miniature mechanisms that form a satellite “tool kit.” Jointly developed by APL and Starsys Research Corp., the mechanisms include a Micro and Mini Separation Nut, a Mini Rotary Actuator, a Micro Burn Wire Release, a Shaped Memory Alloy (SMA) Linear Actuator, and an SMA Redundant Release Mechanism. All of these mechanisms are scalable and show promise for additional miniaturization.

The Mini Separation Nut (mass of 10 g, power of 2–5 W) was designed by Starsys Research to restrain and release a small 0-80 or similar bolt. The separation nut is similar in design to conventional devices in that it is a segmented nut constrained by a collar. With the collar in place, the segmented nut is maintained in the shape of a nut, allowing a mating bolt to be threaded and tightened in place. The collar is maintained in position by a compression spring that prevents the collar from moving because of vibration loads. The collar is driven in opposition to the spring by an SMA element, which is heated directly or can be designed with a resistance heater directly attached to the SMA element. To release the bolt, power is supplied to the heater or SMA element. As it is heated through its transformation temperature, the element recovers previously induced strain and drives the collar to allow the segmented nut to separate, releasing the bolt. When power is discontinued, the mechanism can be manually reset.

The Micro Separation Nut (mass of 10 g, power of 2–5 W), designed by Starsys Research, uses a single SMA band that has been formed into a circular shape. The mechanism is set by inserting the bolt through the housing and past the inner diameter of the SMA spring. The cap holds the SMA spring properly in the housing. The SMA spring is manually compressed from two sides until it is secure around the bolt. The mechanism may now be preloaded and is ready for release. When the SMA spring is heated, it returns to its circular shape, releasing the bolt.

The Mini Rotary Actuator was designed and developed by Starsys Research. It provides 2–6 inch-oz (0.014–0.375 N-m) of torque in two directions over a 120-degree rotational range. The rotary actuator can be used to open and close a small instrument or camera cover and includes a detent latch that can maintain the cover in either the open or closed position without the use of power. The holding torque for either of the two positions is equal to or slightly greater than the output torque of the rotary actuator (2–8 inch-oz; 0.014–0.056 N-m). The design uses an SMA torsion spring wound past its nominal position to rotate the output shaft. As
heat is applied, the spring returns to its nominal position, providing the output torque. This motion drives the output shaft through 120 degrees, at which point the detent will engage. Power is then discontinued and the rotary actuator remains in the open position until the opposite side is operated.

The Miniature Burn Wire Release mechanism was developed at APL for a miniature instrument cover or similar device needing an extremely compact, low-mass, and low-power actuation device. It uses a burn wire to directly carry the tensile load of a cover or screw that is attached to its retainer. Current applied to the wire breaks or fuses the wire at the location of the retainer, releasing the hardware attached to it. This is different from other types of satellite burn wire releases in that this mechanism uses the wire to directly carry the tensile load; therefore, it is a highly simplified design that can be greatly miniaturized. The design can also be easily scaled up or down according to the requirements of the device it is attached to. The burn wire release mechanism has only five components, with one of those released with the cover. These components are also multifunctional. The burn wire is used to hold the mechanism together, carry the restraint load, make electrical connection, and initiate the release action. The size of the wire was based on restraining a 100-g cover. The rest of the mechanism was designed to be packaged as compactly as possible and to provide thread for a 0.060-80 screw. A kick-off compression spring was incorporated to overcome friction.

Linear actuators are prevalent in satellite programs as triggers or switches for mechanical devices. The Mini Linear Actuator being developed at APL is designed to provide a quick-acting, low-shock, linear motion. A single test unit has been built. This prototype mechanism uses SMA wire to actuate a high-force, low-shock pin puller that can trigger a number of latch devices on instrument shutters or covers. It is self-resetable using a bias return spring and can operate in flight for numerous actuations.

The motion (or strain) of typical SMA materials is limited to 8% of the material length. A nominal design for this mechanism would limit strain to 2% to ensure adequate fatigue margin. Larger stroke length can be achieved if room is available across a cover or down the side of a telescope for a longer SMA wire. Redundancy can be designed into the system with dual wires that can be individually powered and can singularly operate the device.

The SMA nickel-titanium wire is directly heated by running current through it. While the device is not too sensitive to its external thermal environment, when heated, its response time can be less than 1 s. Through a strain recovery process in the material, the wire contracts when heated and returns to its original shape when cooled using a compression bias spring. It is a self-latching device that is fully and repeatedly testable.

The Mini Redundant Release Mechanism is designed to provide both electrical and mechanical redundancy. Most mechanisms strive for redundancy in the electrical connections but have single points of failure in the mechanical operation. This mechanism provides multiple redundancies with its ability to operate (release a plunger) with two of the three SMA elements operating. The mini redundant release is in an early stage of development, with one test unit built. This prototype mechanism contains shaped SMA strips that lock a restraint shaft for an instrument cover, solar array, or other system needing a release device. SMA strips grip the end of the shaft while in a cold state. When powered and brought to a higher temperature, the SMA strips change shape to “open the lock.” Full mechanical redundancy is achieved because the device still operates if one of the strips fails to open. A resistor heater on the housing provides the temperature control. This design can be converted to direct current heating to increase the response time. Direct current heating will also provide further electrical redundancy. This mechanism can be miniaturized further depending on the holding force required.
Advanced Thermal Methods for Instruments
Douglas S. Mehoke

Thermal control systems must evolve to adapt to the challenges of reduced mass, size, power, and cost of spacecraft missions. Deep-space mission designs must adapt to a variety of environmental conditions (from Mercury to Pluto) with the smaller bus configurations. Planetary and small-body landers must be able to go into a thermally stable protective mode during periods of low power generation. Traditional spacecraft thermal control systems, using heaters and louvers, have high resource costs (power, mass, cost, and complexity) that make them unusable for these new types of missions. To support the next generation of missions, the ATD program has developed the Miniature Spacecraft Energy Retention (MISER) panels as a low-power, low-mass, and low-cost alternative for spacecraft thermal control.

Over the past 2 years, the ATD program, working with Starsys Research and Virginia Tech, has been developing a thermal control panel that uses a spacecraft's internal power to control its temperature. The panel incorporates three different thermal technologies: a thermal switch, a high-conductivity composite radiator, and a tailorable thermal control surface. These technologies are combined into a modular system that can be readily adapted to different structural configurations. The MISER panel provides a flexible thermal control option that will allow significant new options into future missions.

MISER heat switch
- maximum conductance = 0.46 W/°C;
- heat switch minimum conductance = 0.0043 W/°C;
- heat switch conductance ratio = 107:1;
- radiator area = 8.5 × 8.5 inches (21.6 × 21.6 cm);
- overall power turndown ratio = 20:1.

Within the MISER panels, the gap closes when the paraffin expands (upon melting), creating a good conduction path to the radiator.
A reliable thermal switch is the key to the MISER panel. While thermal switches have been used before, the design and test costs associated with each new design make them an undesirable alternative. The MISER panel incorporates a fully tested thermal switch with a radiator into a modular system that can be easily added onto any spacecraft structure. The assembly remains unchanged between different mission applications, providing the cost saving and proven reliability that are the key to using this type of technology.

The thermal switching action is powered by the phase change properties of paraffin. When paraffin melts, it expands by about 15%. This volume change is used to bring two thermally conductive surfaces into contact, creating a path through which heat can readily flow. Several different types of paraffin are available that allow the switching temperatures to be set between –95°C and 86°C. The switch for this study was charged with 18°C paraffin.

The variation in the thermal conductance of the switch in the conducting and non-conducting states was measured and found to be greater than 100 to 1. The temperature difference was taken between the switch baseplate and the radiator. The maximum conductance achieved was 0.46 W/°C; the minimum conductance was 0.0043 W/°C. The switch is designed to provide a controlled temperature for power variations between 0.5 and 10 W.

The switch has a demonstrated lifetime necessary for long-duration space missions. The switch design uses a static seal to reduce the possibility of leakage. A lifetime test was performed on the seal design with the seals being mechanically flexed over 100,000 cycles. The switch/radiator assembly was life tested as a unit to over 60,000 cycles.

The lightweight radiator makes the MISER panel self-supporting, so interfaces with the mounting structure are simplified. Composite radiator panels with highly conductive materials can be made very thin, which reduces their mass and allows more flexibility in their application. The use of fibers with very high thermal conductivity and filters designed to locally improve the through-panel conductivity makes these radiators practical.

Preliminary work on a new thermal control coating would make the panel less sensitive to the orientation of the Sun. By changing to a hotter coating, the panel could be used as a power-free heater for deep-space missions. The same panel provides thermal control over a wide range of environmental conditions, making constellation spacecraft viable with significantly different orbits.
Resonant Laser Methods for Instruments

William B. Brinckerhoff and Timothy J. Cornish

Future in situ science missions to planets, comets, asteroids, and planetary moons will require significant advancements in miniaturized sample analysis technology. For both in-depth scientific studies and sample-return reconnaissance, the composition of a wide range of materials must be analyzed in detail. Examples of desired measurements include microprobe elemental analyses from a small field of view, high-precision isotope ratios of key volatile and refractory species, and identification of large organic molecules. The Resonant Laser Methods effort at APL has focused on enabling such composition studies through the development of miniature optical parametric oscillator (OPO) laser techniques. The technology readiness level advancement of OPO laser probes from concept phase to test phase is a critical step in achieving the most challenging sampling mission goals.

The advent of efficient, compact, rugged lasers has improved the prospects for such sensitive in situ analyses. Miniature solid-state lasers, such as Nd:YAG, and semiconductor lasers (laser diodes) are finding their way into a variety of spacecraft instruments for spectroscopy, ranging, and referencing. For composition measurements on landed missions in particular, lasers and associated optical coupling systems can perform three main functions:

1. Volatilization, or removal, of particles from samples
2. Excitation of molecules for absorption, Raman, or fluorescence spectroscopy
3. Ionization of excited species for detection by mass spectrometry

In some applications, such as laser ablation mass spectrometry, a single, pulsed laser is used for all three functions. The laser first removes particles from a spot a few micrometers in diameter on a sample by ablation, and then excites and ionizes them in the high-density plume that forms above the sample. Many analyses, however, require sensitivity and selectivity unreachable with combined methods. One example is the detection of trace elements, i.e., those present in a sample at levels only from about 10 parts per million (ppm) down to 10 parts per billion (ppb) by weight. The lanthanide elements and certain high-mass metals such as In, Sn, Ir, Pt, Au, and Pb are important indicators of planetary thermal processing but are expected to occur only at levels below 100 ppb on Mars, asteroids, and comets. These are very difficult to detect and quantify with single, fixed-frequency laser methods; the excitation and ionization processes are optimized at very different laser parameters from those for the volatilization step. Similar arguments apply to organic molecules, which may also occur only at low levels.

To overcome this limitation in miniature in situ instruments, the Resonant Laser Methods ATD effort at APL has focused on the technique of post-ionization, or excitation and ionization by a laser applied after the sample is vaporized. By decoupling volatilization from subsequent steps, the exciting laser wavelength can be tuned to match energy-level transitions of a specific element or molecule, “selecting” it for detection.
with much higher sensitivity than other “background” species. The selective ionization of one element can also reduce same-mass, or isobaric, interferences among isotopes and molecules, without requiring extremely high mass resolution (and the typically large, power-hungry instrumentation associated with it). While miniaturizing this resonance ionization technique is a significant challenge compared to fixed-wavelength spectroscopy, there is a critical long-term need for a broadly tunable, high-power excitation and ionization source to enable sensors for compounds of which the identity and abundance is not known \textit{a priori}.

The technology used to obtain tunable laser light in this effort is a miniature OPO. The OPO is a passive nonlinear optical device that converts an input, or pump, laser into two discrete beams, signal and idler, with photon energies that sum to the pump energy. The signal wavelength is tuned by rotating the OPO’s birefringent nonlinear crystal within a resonant cavity. By pumping the OPO with 355-nm light from a Nd:YAG laser, we obtain tunable output across the visible range (410–690 nm). Frequency doubling expands the available range to include near-ultraviolet (UV) light, which is optimal for excitation of many elements and organic molecules. The OPO method has distinct advantages for potential \textit{in situ} instruments over alternative techniques such as dye lasers, tunable diodes, and Ti:sapphire lasers in that it can provide high energy, high efficiency, and broad tunability in a compact and relatively rugged package. The OPO used in this project is a unique, highly miniature design by Opotek, Inc., of only a few centimeters on a side.

We have investigated a range of OPO-enabled optical instrument sourcing and coupling schemes for resonance excitation and ionization. In the simplest scheme, the OPO output was coupled to a sample surface at normal incidence through a long-focal-length ($f = 25$ cm) athermal objective system, simultaneously adjusted for beam divergence and spot size over the wavelength range. Neutral particles were volatilized and ionized with direct OPO laser desorption and then analyzed in a time-of-flight mass spectrometer. A resonant laser ablation effect was observed by scanning the OPO wavelength. We found that, with a highly confined ion extraction region, normal incidence was simpler and more sensitive than glancing incidence. This is in contrast to what has been found in larger, laboratory-scale instruments.

We have designed and compared two geometries for post-ionization in compact instruments. In the \textit{lateral} geometry, the fiber-coupled OPO output was directed parallel to, and slightly above, the sample surface, at an adjustable delay (around 1 $\mu$s) following an initial, normal-incidence desorption pulse from a separate laser. This geometry is similar to that used in standard resonance ionization spectroscopy and gives the best control of plume overlap. In the \textit{coaxial} geometry, the OPO output shared the objective system of the desorption laser, but was again focused to a point just above the sample. When the desorption wavelength was longer than the OPO wavelength (e.g., the 1064-nm Nd:YAG fundamental), we found that the OPO focus height could be continuously varied over 1–2 mm by using the intrinsically slightly shorter focal lengths of the visible and UV light.

Initial post-ionization mass spectra of metal foil and thin powder samples in the 410–500 nm visible range demonstrated the feasibility of coupling the resonant laser technique to miniature instruments. Promising results were achieved in both geometries with minimal hardware, though the coaxial post-ionization method would lead to the most compact microprobe instrument. However, the lateral geometry avoided the problem of unwanted delayed desorption by the OPO, a consequence of the extended OPO beam waist region at long coaxial focal lengths. Significant savings in mass and power could also be achieved by splitting the output from a single laser source. One beam would be used for volatilizing the sample and the other for pumping the OPO. We found that, in some sample series scans, a fixed two-pulse delay of just under 1 $\mu$s gave satisfactory results across a well-defined range of elements. As such, it is feasible to consider a high-transition fiber optic spool of fixed length (approximately 175 m) to provide the required delay without a second laser source and delay electronics.
As space exploration becomes more ambitious and focused, robotic and piloted missions will increasingly rely on sophisticated analytical tools, which may require precise manipulation of samples and high vacuum conditions to operate. Examples include mass spectrometers, electron microscopes, and x-ray diffractometers. These requirements are readily met in laboratories by incorporating commercial inlet systems and vacuum pumps into the instruments without excessive concern for their incremental demands on power, mass, or space. While such an off-the-shelf approach is highly attractive for developing similar systems for spacecraft at low cost, miniature sample and vacuum systems (SVSs) for use in extremely resource-limited and harsh environments have only begun to be developed.

For missions to bodies without atmospheres, a vacuum pump may not be needed, and it is possible to analyze solid materials to some degree without handling the sample. For instance, a laser can directly remove and ionize particles from a small spot on the surface, which can then fly unhindered through a mass spectrometer for elemental and isotopic analysis. Even on bodies with significant atmospheres, such as Mars, Venus, or Titan, some composition information can be obtained with spectrometers that detect reflected radiation rather than ions. These types of sensor do not require SVS hardware either. For instance, the APX spectrometer on Mars Pathfinder was simply placed against a sample of interest for bulk analysis.

However, many high-precision instruments will require a sample handling system to work with small solid samples. This is primarily because of the need for careful focus control: microscopes, laser and ion beams, and other probes must be brought into three-axis alignment, possibly simultaneously, to analyze structure within and among mineral grains. It is usually easier to get this precise control (in a miniature, rugged package) by manipulating the sample than by positioning multiple probe heads, lenses, mirrors, or the instrument arm itself. When there is an atmosphere, precision vacuum techniques additionally require a pump to attain low pressures (typically $P < 10^{-6}$ torr). Then the sample handling system must also provide a means to transport the sample through a vacuum lock, which can simply be a sealed door to the entire instrument that would be vented for each new sample. But this is almost never done in practice. One generally goes to great lengths to avoid re-pumping out the entire apparatus from ambient pressure, and in laboratory instruments this is done with motion feedthroughs, sample transfer mechanisms, and differentially pumped load locks. The pressure tolerances, outgassing properties, and range of motion of these components must be matched to the capabilities of the pumping system and needs of the instruments enabled by the SVS.

In this SVS ATD effort, we have developed designs and hardware to enable the acquisition, vacuum insertion, manipulation, and positioning of small solid samples (from dust to small rock or ice chips) for in situ landed instruments. The focus on this size range has been motivated by the need for micro-
scale analyses of unprocessed samples (such as grain composition for mineralogy), balanced by the need for multi-sample vacuum insertion and the realities of limited power and mass resources. In partnership with Creare, Inc., we have also furthered the development of ultra-miniaturized, low-power turbomolecular pumps (TMPs) for remote operation by both testing an initial TMP prototype under realistic instrument conditions and designing an enhanced version for operation on Mars with no backing pump. All SVS hardware components we developed are significantly smaller and lighter than the high-capability instruments they enable, providing a new, more optimistic view of the potential for a high level of in situ capabilities.

An example of the sample acquisition and manipulation systems developed is the rotating probe wheel prototype. This device acquires fine particles such as those from loose regolith or the output of a rock drill or chipper, and positions them in vacuo for analysis. In one tested implementation, the probe wheel is fitted to the sample end of a microprobe instrument at the end of an articulated robot arm. A probe rod 3 mm in diameter extends from the wheel housing, through a shield, and toward the sample. The probe tip supports any of several possible sample-grabbing mechanisms. One simple design that works very well with fine particles is an array of grooves laser-etched in a silicon substrate, with widths ranging from 10 to 50 μm and a depth-to-width ratio of about 1.5. Light pressure of the probe-mounted substrate into a pile of loose, unsorted JSC Mars-1 simulant ash is sufficient to nearly fill the grooves with a range of grain sizes, with little volume loss on retraction.

The probe tips are extended by means of small shape-memory alloy (SMA) springs seated in the wheel wells, offering an excellent low-power, small-volume solution for precision placement. A standard bias spring retracts the tips when SMA power is removed. With probes in the retracted position, the wheel is free to rotate past a sequence of O-ring seals until the chosen probe is in the analysis position (nominally opposite the sampling position). The probe is then re-extended, making a second-level surface seal with a high-vacuum valve. In the analysis position, the grooves provide the substantial added benefit of strongly localizing the grains for analysis. For instance, highly reproducible laser mass spectra were obtained that could not have been obtained without such micro-confinement.

The ultra-miniature TMP is used to bring the analysis space of the acquired sample to pressures below 10⁻⁶ torr. TMPs are an excellent choice for instruments in planetary survey scenarios where multiple samples will be inserted and studied in sequence to capture spatial composition trends. Within a pump housing volume of less than 200 cm³ (m < 400 g), the TMP achieves pumping speeds above 4 L s⁻¹ while drawing less than 1 W. A design lifetime of over 1 year is achieved at a rotational speed of 10⁵ rpm. As a throughput pump, the TMP performs extremely well during initial pump-down and easily handles the pressure transient generated by pulsed thermal or laser evaporation methods (expected to degrade performance of capture pumps over mission lifetimes).

Starting from analyses of initial tests and a range of possible instrument configurations, a design for an enhanced mini-TMP with drag stages has been developed that will operate at Mars ambient without a backing pump. The higher exhaust pressure tolerance of 10 torr increases the power draw of the TMP itself, but the mass and power requirements of the total vacuum solution for Mars are minimized.
The ATD program has examined the ability of a liquid crystal tunable filter (LCTF) to function in space; in particular, the program has been defining its response to radiation. The VariSPEC™ LCTF developed by Cambridge Research & Instrumentation can selectively transmit light of a specific wavelength using controlled electrical signals to allow rapid, vibration-free selection of any wavelength in the visible and near-infrared range. A controllable, swift, and motionless selection of wavelength enables multi-spectral, high-resolution images using monochrome charge coupled device cameras, making the LCTF potentially valuable for a spaceflight instrument.

The commercial LCTF used in these tests had a clear aperture of 20 mm and a spectral bandwidth of 10 nm, and it can be tuned to any wavelength in the range of 400–720 nm.

The tests performed consisted of measuring the transmission of the LCTF and its individual components, and measuring the degradation of the transmission as a function of the radiation dose. Measurements were made with the filter set to wavelengths of 450, 500, 550, 600, 650, and 700 nm. Radiation doses started at 1 krad and were gradually increased to 20 krad until the total dose was 71 krad.

For the LCTF tests the filter was tuned to wavelengths of 450, 500, 550, 600, 650, and 700 nm, which spanned almost its full range of 400–720 nm. The LCTF successfully filters other wavelengths within its spectral range, but the transmission does increase above a wavelength of 780 nm so caution is necessary when using the filter with a broadband source and detector. The filter provided a smooth symmetrical profile at each wavelength. LCTF peak transmission increased as the wavelength setting increased. Before receiving radiation, the LCTF transmission increased from 7.56% when tuned to 450 nm up to 38.94% at the 700-nm setting. The absolute values are affected by the polarization of the input beam.

To study changes in LCTF transmission, we compared these maximum values, or peak LCTF transmissions. A total dose of 71 krad of radiation caused peak transmission at 450 nm to drop from 7.6% to <1.5%. At 700 nm the transmission fell from 39% to 28% with 71 krad of radiation. Typically, for wavelengths above 500 nm the absolute transmission fell by about 12%. This corresponds to a transmission reduction rate of approximately 0.17% per krad of radiation. This rate tended to be slightly higher for settings in the middle of the visual spectrum and lower for those near the edge. For doses up to 31 krad, the rate of decline at the 450-nm setting resembled the rates of decline at the higher wavelength settings. After 31 krad, 450-nm LCTF transmission declined more slowly and seemed to approach a minimum value somewhere between 1% and 2%. The transmission declined more slowly at all wavelengths for doses approaching 71 krad.

In general, radiation affected the LCTF more than the individual components and it left the polarizer transmission virtually untouched. Radiation caused the LCTF transmission to decline an average of 0.16% per krad. Visible component transmissions declined at rates comparable to LCTF decay rates only near 400 nm. At longer wavelengths, visible component transmissions declined at relatively insignificant rates of less than 0.02% per krad. In comparison, polarizer transmission diminished less than 0.05% per krad along the whole visual spectrum and diminished only 0.025% per krad on average. Between doses of radiation, transmission generally recovered no more than 0.5% per day if it recovered at all. By and large, annealing effects were small and insignificant in comparison to drops in transmission caused by exposure to radiation.
The trend toward deploying constellations of ever-smaller spacecraft, including nanosats and picosats, to characterize ionospheric features will require new miniaturized plasma spectrometers with a high ion throughput-to-volume ratio. Constellations of small spacecraft with these instruments on board would enable simultaneous measurements of energetic charged particles from many different vantage points. The current lack of miniaturized, yet sensitive, charged-particle spectrometers is being addressed by a collaborative effort between NASA Goddard Space Flight Center, The Johns Hopkins University Applied Physics Laboratory, and the College of William and Mary. The goal of the first phase of the program is to develop a prototype flat plasma spectrometer (FlaPS) to measure the energy and angular distributions of ions ranging from 10 eV to 10 keV in a space environment. The second phase will focus on developing and flying the FlaPS hardware as a small payload deployed by the space shuttle. The concept for the flight-ready FlaPS system envisions multiple detector elements arranged in a cylindrical pattern around the spacecraft, providing a 360° field of view with 5° angular resolution.

To validate the feasibility of the miniaturized instrument, we are examining the design, fabrication, and performance issues of a prototype spectrometer. A preliminary design for a prototype device has been developed and built that includes a collimator, deflector electrodes, and a detector. The collimator consists of a stack of many parallel apertures that were micromachined with deep reactive ion etching of silicon wafers. The wafers are mounted above a series of interdigitated copper deflector electrodes that have been microfabricated by electric discharge machining. The detector resides below the collimator/deflector assembly. This element includes a matched pair of microchannel plates coupled with a position-sensitive detector. In this configuration, the prototype instrument essentially consists of a large number of parallel particle analyzers. The active region of the device occupies a volume of about a cubic centimeter.

The initial design for detecting and analyzing ions involves spatially resolving energy-to-charge ratios of particles exiting the deflector plates with an amplifier/detector combination consisting of the microchannel plates and a resistive anode. To achieve maximum sensitivity, the deflector plate voltage will be stepped. By using a one-dimensional detector with 50-μm spatial resolution, we expect that particle energy-to-charge ratios can be measured with up to 4-bit resolution per deflector plate voltage step.

The first-generation prototype has been fabricated and assembled and is being evaluated in an ion beam facility at the College of William and Mary. The results will be used to design and test advanced FlaPS prototypes. Ultimately, we hope to integrate this technology with a series of nanosats to further characterize charged particles in the ionosphere.
Autonomy

The Advanced Technology Development (ATD) Program’s investigation into autonomy technologies has focused on important strategic technical challenges facing space exploration: the reduction of mission costs, the continuing return of quality science products through minimal communications bandwidth, and the launching of a new era of exploration. Because of the growing number of on-duty spacecraft, plus those set to explore the solar system in the next decade, the Deep Space Network (DSN) will face a communication overcrowding problem. New techniques and systems are becoming increasingly desirable to free up the DSN and associated mission control centers from time-consuming tasks. APL is developing innovative, efficient autonomous systems for the selective migration of operational functions to the spacecraft, and new onboard software architecture and operating concepts to integrate these functions.

Autonomous Navigation

APL is endeavoring to enable a spacecraft antenna to point to Earth without the need for uplinked ephemeris data, which will reduce DSN resources required after a period of spacecraft hibernation, potentially allow for autonomous thruster firing as part of autonomous navigation, and complement optical navigation by the spacecraft. For precision orbit determination, one-way Doppler measurements made onboard a spacecraft will enable spacecraft autonomy to develop an accurate navigation solution. We are working to characterize the errors in one-way Doppler measurements as a function of time since the last characterization of the spacecraft oscillator. This involves the adoption of a model for oscillator drift over time and temperature.

The autonomous navigation system is a self-contained system that uses the Sun as the navigation reference body and determines the spacecraft’s orbit using observational data acquired and processed onboard the spacecraft. Since the Sun is always visible, even during the long interplanetary cruise phase when other usable reference bodies are very limited, this system is better than systems that use asteroids as reference bodies. It has the potential to guide spacecraft voyaging anywhere in the solar system—to asteroids, comets, and our most distant planets.

APL investigated an autonomous navigation system using the Sun as the navigation reference body by analyzing cases of various mission trajectories and navigation requirements. An orbit determination strategy and algorithm, as well as orbit determination software programs, have been developed. Navigation accuracy using different data types—solar data alone or solar data in combination with other onboard measurements—was also studied.

Autonomy Architecture

Spacecraft hardware and software are designed to provide an extraordinary level of fault tolerance. There needs to be a system that can save the spacecraft, establish communication with the ground, and return the spacecraft to an operational mode. The ATD Program’s new safing architecture will perform that function. The APL Integrated Electronics Module (IEM) intends to

The far side of asteroid Eros looms like an enormous wall beyond a near horizon in the foreground.
Man–Machine Interaction

The ATD Program is developing an environment that will support rapidly building flexible remote access systems for test or operational data. Such an environment will significantly lower the cost and increase the effectiveness of providing spacecraft data to scientists, engineers, and students. In particular, scientists will be able to interactively select data streams, choose and configure filters to be attached to the streams, choose and configure graphing and display objects to be attached to the results, and save the setup for later use, all without any explicit programming.

The ATD Program is also developing user interface designs, information architectures, and software components that can support users’ interaction with autonomous spacecraft. Autonomy research efforts have focused primarily on system architectures, software architectures, and software components for autonomous spacecraft operation. Future mission use of these capabilities, however, will also depend critically upon the mechanisms by which Earth-based mission operations and science teams interact with advanced autonomous spacecraft. Successful dialogue between the spacecraft and its users will depend upon the ability of users to understand important relationships among goals, constraints, and particular states of the spacecraft, of its environment, and of the science data that it is measuring, summarizing, and communicating. Operations and science personnel will require information access and display capabilities that quickly and easily portray spacecraft state, history, goals, and plans in relation to each other and at various levels of granularity. We are developing prototype user interaction mechanisms that include elements of both the user interface and the underlying software layers that mediate between users’ information representations and the software information representations appropriate to spacecraft systems and autonomous agents that manage them.
Autonomous Interplanetary Navigation

The orbital elements \(a, e, \) and \(i\) can be determined by the spacecraft's orbital angular rate \(\dot{\theta}\) via observation of the Sun's direction as a function of time, with additional orbital elements \(\Omega, i, \) and \(o\) determined by the Sun's direction vector \(\mathbf{n}\). Navigation plays a critical role in deep space missions since a spacecraft launched to a planet, asteroid, or comet must be accurately navigated to reach its destination in a close flyby with, orbit at, or landing on the targeted body. Autonomous spacecraft navigation is desirable for future space missions, especially for missions that require updates of a spacecraft’s position in real time. Autonomous navigation can be used to approach small planetary objects, such as the asteroid Eros. It can increase a spacecraft’s capability and flexibility, taking immediate action in critical situations without any two-way light time delay, thereby increasing the spacecraft’s survivability and reducing risk. It also reduces mission operation costs. We are developing a self-contained, autonomous navigation system for interplanetary missions. The navigation system uses only onboard observations of the Sun in combination with the onboard spacecraft attitude data to estimate and predict the spacecraft’s orbit autonomously. Unlike the current ground-based navigation system, which uses two-way coherent radio Doppler tracking through the Deep Space Network, the new system does not need the Deep Space Network or any control from the ground. The system has the great potential to guide a spacecraft anywhere in the solar system, even to nearby stars.

By means of solar navigation the spacecraft determines its orbit from onboard observations of the Sun using instruments that may already be carried for other purposes. This navigation method is unique in that it is completely self-contained and universally applicable. The self-containment allows the spacecraft to navigate independently without relying on signals transmitted from the Earth. Since the Sun is an active energy source and visible everywhere in the universe, this navigation system of using the Sun as a navigation reference is applicable to spacecraft moving anywhere in space.

The spacecraft's state (its position and velocity vector) is determined by processing the solar observation data on board. Two types of solar data may be used for estimating the state of the spacecraft:

1. The directional data that measures the change in the Sun’s direction as a function of time, viewing the Sun from the spacecraft against the star background.
2. The optical Doppler shifts observed in sunlight that provide the line-of-sight velocity of the spacecraft relative to the Sun.
Through an analytical derivation, we have proved, in general, that all six orbit elements (equivalent to the six components of the spacecraft's state) that define a spacecraft's orbit can be completely determined with measurements of the Sun's direction vector as a function of time. The use of optical Doppler data in addition to the directional data, though optional for orbit determination, adds a constraint in the dimension perpendicular to that given by the directional data. Inclusion of the optical Doppler data in the orbit determination process can speed up the convergence of the orbit-fitting process and improve the orbit solution.

We have made a conceptual design of a dual-mode imaging system that measures the Sun's direction using a charge-coupled device camera by capturing the image of the Sun against a background of stars. The stars appearing in the Sun's image frame serve as a direction reference. The conventional optical imaging system, which is designed for imaging planetary bodies, cannot be directly used for taking the Sun's image because the Sun is much brighter than the planetary bodies. Our design modifies the conventional optical imaging system by controlling the intensity contrast of light coming from objects with large differences in brightness. The designed image system can take pictures from both planetary bodies and the Sun by operating in two modes: as a regular imager when imaging planetary bodies or as a Sun imager when imaging the Sun.

We developed an algorithm and a software program for numerically determining the orbit of spacecraft using the least squares method to fit the orbit parameters with the solar directional data. We also developed a suite of software programs for modeling and simulating the performance of the solar navigation system. Navigation accuracy can be analyzed by simulating the observation data based on realistic spacecraft trajectory and measurement error models. The truth model of the spacecraft orbit used in simulations is generated by numerical integration on a high-precision gravity model that includes the perturbations of third bodies.

The practicality and feasibility of using solar navigation was assessed by applying it to a real space mission. We selected the Solar-Terrestrial Relations Observatory (STEREO) mission as our case study because its available onboard science instrument (the Solar Coronal Imaging Package) can measure the Sun's direction with no additional hardware being required. The STEREO mission, which will be launched at the end of 2004, will provide a new perspective on solar eruptions (coronal mass ejections) and their consequences for Earth by imaging the ejections and background events from two spacecraft simultaneously.

We simulated an orbit determination based on the mission trajectory profile and onboard instrument and system capability for the STEREO mission. Sun direction measurement errors contributed from the science instrument and the guidance system were considered and folded into the simulated observation data. We used the simulated Sun direction data to estimate the spacecraft's position and velocity vector. Orbit estimation errors were derived by comparing the estimated values with the truth model.

The results from the simulations performed on STEREO show that an orbit solution better than ±200 km can be achieved by solar navigation using the available onboard science instrument and the guidance and control system. It is well below the mission required uncertainty limit of ±7500 km. A two-way coherent Doppler tracking navigation is baselined for the STEREO mission. We proposed an in-flight test of a prototype of a solar navigation software package on the STEREO mission. If it proves to be reliable in the test, the solar navigation system can serve as a backup for the remaining mission time.

Solar navigation has demonstrated real space mission feasibility and comparable navigation accuracy with current instrument technology in the studied cases. Given its unique ability, self-containment, and universal applicability, benefiting from the technology development and innovation in instrument and sensors, autonomous solar navigation is very promising and has great potential for enhancing spacecraft performance in space exploration.
This ATD project explored the use of one-way Doppler measurements to aid in spacecraft navigation. One-way Doppler measurements may be made on board a spacecraft and then telemetered to the ground in order to shorten the time necessary to determine a navigation solution. This may be especially useful following a cruise phase period during which no two-way Doppler observations are made. The one-way Doppler measurements would be made on board a spacecraft based on the presence of a beacon transmitted from a small (e.g., 10-m) ground antenna. The basic concept is shown in the accompanying figure. The benefits of this project are a reduction in Deep Space Network resources required after a period of spacecraft hibernation. The goal is to establish the practicality of removing spacecraft oscillator drift and obtaining proper time registration of the resulting data for use in ground processing.

Analysis of historical oscillator data indicated that errors of a few parts per billion must be tolerated over a 6-month period. The data used for this analysis represented about 15 Oscar navigation spacecraft over a 30-year interval.

The primary issue addressed is correct registration of the on-board measurements with the ground clock without reference to an accurate real-time clock on the spacecraft. It is assumed that the spacecraft oscillator frequency is measured through two-way observations before and after the cruise interval. In this way, the average drift of the spacecraft oscillator can be removed from the problem. It is also assumed that a rough range estimate is available for use in analyzing a given pass. A range precision that provides an accuracy of 1 ms in the one-way light time is sufficient (i.e., 300 km).

Before the beginning of the cruise phase, two-way measurements are made of the spacecraft range, Doppler velocity, and reference oscillator frequency. Spacecraft range can be measured by standard methods, which include sequential ranging tones and pseudo-noise codes. The Doppler velocity and reference oscillator frequencies can be determined through the use of the APL noncoherent navigation hardware and methods. No new development is required for these measurements.

One-way Doppler data will be created during all, or selected, ground station passes. During each measurement pass, the ground station will transmit an unmodulated carrier at a frequency that is tied to the ground system clock. At one or more times during the pass, the uplink frequency will be changed. The precise time of these frequency changes will be recorded. The spacecraft will count uplink phase and reference oscillator phase. It will make periodic measurements of the phases and store them in memory.

After the cruise phase, two-way measurements of the spacecraft range, Doppler velocity, and reference oscillator frequency are made as they were before the cruise phase. The on-board measurements are telemetered to the ground. The two-way measurements from before and after the cruise phase are processed with the one-way on-board measurements to determine the spacecraft Doppler velocity throughout the cruise phase.

The spacecraft oscillator frequency is known at the beginning and end of the cruise phase through direct, two-way measurements. The average frequency over the cruise phase is known as well from the cumulative phase change observed by Bob Jensen
the spacecraft over the cruise phase. This is equivalent to an observation of the elapsed spacecraft time during the cruise phase. These three pieces of data are sufficient to develop a cubic drift law for the spacecraft oscillator over the cruise phase. This drift law will not be perfect, but it will remove the bulk of the uncertainty due to oscillator drift.

The change of the uplink frequency during a given pass occurs at a known time on the ground. It is necessary to establish the spacecraft time corresponding to the observation of this frequency change. This process is performed in two steps. In the first step, the measurement interval during which the change occurs is determined by observation of a discontinuity in the uplink frequency. In the second step, a polynomial fit of the uplink phase is made based on points before and after the interval of interest. The point of intersection of these two fits is the time of the frequency change.

Given an uplink interval, we wish to establish the Doppler frequency observed by the spacecraft. This observation will be delayed by the one-way light time. Relative to the frequency change time, the uplink phases at the beginning and the end of the uplink interval are known. These phases, relative to the phase at the frequency change time, are equal on the ground and on the spacecraft. We therefore know the uplink phases observed by the spacecraft that define the uplink interval of interest. By interpolation of the telemetered data, we can precisely determine the spacecraft reference phase at the beginning and end of the uplink interval. These are combined with the oscillator drift law established previously to determine the uplink Doppler frequency.

Conventionally, Doppler velocity is measured over a given downlink interval. We can establish an effective downlink measurement through an iterative procedure with the use of an approximate value of the one-way light time between the spacecraft and the ground station. Given a rough knowledge of the range between the ground station and the spacecraft, it has been established that the velocity measurements may be translated into one that applies to a given downlink interval of time. A range precision of 300 km suffices for this purpose.

It is possible to precisely determine the spacecraft Doppler velocity based on measurements made by the spacecraft and stored for inclusion in telemetry following the cruise phase. The on-board measurements can be tagged to a specific uplink time by the use of a frequency step in the uplink.

Simulations of the approach described here have been performed to determine the Doppler accuracy that can be achieved. An example of the results shows that Doppler velocity precision at the level of less than 0.1 mm/s can be supported, even in the presence of oscillator drift rates of 3 parts per billion (ppb) over a 6-month interval. Since this is the level of performance achieved by two-way transponder measurements, the one-way measurements made during a cruise phase can be used in place of such two-way measurements. Therefore, valuable resources that would be required for these two-way measurements are saved.

http://sd-www.jhuapl.edu/ATD_NASAAPL/
Subobject Tracking and Proximity Operations
Gene Heyler

While much of the capability to autonomously detect, track, and hand over to a narrow field-of-view (FOV) sensor was demonstrated on the Midcourse Space Experiment (MSX) spacecraft with the UVISI instrument, the goal of this ATD project is to develop a system that can process images on board the spacecraft to autonomously acquire and track unresolved point-source objects such as asteroid sub-satellites or cometary fragments.

This enhancement would enable automated satellite and object searches to be performed, i.e., the spacecraft would autonomously distinguish between inertially stable stars and moving objects. On board track processing would develop tracks on those moving objects and provide estimates of their trajectories based on the optical reports. Initial acquisition could take place in a wide FOV acquisition sensor and, once firm track is established, the track could be handed off to a narrow FOV, higher-resolution tracking sensor. As a by-product, the onboard image/track processors will be able to detect and report identified stars to augment the capabilities of an onboard star tracker guidance system. A long-term goal would include the ability to use the sub-satellite/cometary fragment tracking information for collision avoidance maneuver planning.

Most near- or deep-space satellite probes require significant ground support to choreograph observation events. By having an image/track processor suite on board, much of the detailed pointing control of the satellite would be offloaded from the ground operations. The satellite could be given a coarse cue of where to look for the object; it would then autonomously acquire, track, hand over to a high-resolution sensor, and point the spacecraft at the object of interest, thus optimizing data collection. Such a system would not only be advantageous when scheduled observations are performed but would also provide the ability to discover new comets or asteroids using the satellite/object search algorithms. The system would be designed such that the onboard image processing algorithm suite can incorporate the capability to identify regions of interest during rendezvous or flyby and extract features of resolved objects (such as craters); this would expand the system acquisition and tracking capability to include resolved geologic features as well.

Initially, this project analyzed work done on planetary body size estimation, autonomous onboard image mosaic planning, and automated resolved feature detection using Gabor filters. Subsequently, the focus of the ATD work was on...
the rather challenging image processing techniques required to extract the information from the imagery of the resolved objects. Aspects of the problem that were not addressed earlier included stability requirements and algorithms used to track either the object’s center of mass (far-encounter geometry) or the resolved object’s features (near-encounter geometry). APL’s expertise in Kalman filtering and state estimation were important for improving this work.

To further this ATD effort’s immediate goals of developing an onboard system to detect and track point-source or small extended objects, we drew on the image processing algorithms developed in support of other programs such as MSX, NEAR Shoemaker, and FUSE. For MSX we developed an onboard image processor that could detrend the data, threshold out candidate targets, collect the useful feature information (including centroids), and report the top 23 candidates to the onboard tracking processor. This algorithm worked successfully on orbit to track various objects and satellites. The algorithms developed for NEAR Shoemaker were ground-based analysis routines designed to perform a satellite search around the asteroid Eros. These algorithms were tested and refined on the asteroid Mathilde flyby dataset and run in C and IDL. Perhaps the most evolved code is that being flown on FUSE. This algorithm uses a spatially adaptive threshold to segment out stars from the background. Extended objects as well as point sources are detected; the algorithm works on up to 520 × 520 pixel arrays but can easily be modified to work on larger images.

The salient outputs from this algorithm are the centroids of each object detected. Other ancillary information is also provided, such as the size and intensity of the detected object. Additional shape information such as eccentricity and the lengths of semi-major and -minor axes are not computed in the FUSE code but were part of the original MSX code. However, the algorithm is not sophisticated enough to be able to detect features on extended objects like craters or mountains; the Jet Propulsion Laboratory’s (JPL’s) algorithms for feature detection, for example, using Gabor filters, could replace the FUSE-based algorithm for feature tracking events. We envision the two algorithms, APL’s point-source detection and JPL’s feature detection, being arranged in parallel with one or the other being run depending on the type of tracking event planned. The outputs of either algorithm will be transmitted to the tracking software, which will perform the data association, develop candidate tracks, and estimate state vectors.

An algorithm for determining the orbit parameters of possible moonlets of an asteroid based on a sequence of three angle-only optical sightings was programmed and tested. The algorithm is based on equations originally published by Laplace for determining the orbits of comets and planets. It requires no a priori information and can be used as a starter for a Kalman filter algorithm, which would use additional angle-only measurements to refine the initial orbital estimates and reduce error in those estimates.

Specific autonomous subobject tracking and avoidance efforts progressed to the point where we developed the software, which could be demonstrated, for actual autonomous operations—a controlled approach by NEAR Shoemaker to Eros. This would include evaluation of ground testbed hardware (an engineering model of the laser rangefinder) and flight software and uplink of that flight code to NEAR Shoemaker.

At the conclusion of the 2-year ATD project, the APL language simulator, developed for testing other navigation and estimation algorithms, was ported to a second PC platform, and an algorithm for determining the orbit parameters of possible moonlets of Eros, based on a sequence of three angle-only optical sightings, was programmed and tested. Baseline Matlab graphics functions were coded as a precursor to developing a visual animation of subobject tracking, and several orbit utilities were recoded from the APL language into Matlab. Further, a test on the brassboard of the NEAR laser ranger data interface to the NEAR flight computer was successfully completed.
The ATD program’s version of a thinking spacecraft and intelligent ground system comes together to complete the puzzle for an autonomous mission.

The goal of an autonomous system is to perform on its own, end to end, with little or no direction from operations and scientists, i.e., an intelligent mission. Our concept is a thinking spacecraft and intelligent ground system coming together to complete the puzzle for an autonomous mission. We have researched autonomous architectures and identified technologies necessary to achieve the goal. Various organizations are developing critical technology that can contribute to achieving the goal; for example, the Jet Propulsion Laboratory (JPL) is developing the Mission Data System (MDS). We are leveraging the work being performed on autonomous architecture at different NASA centers and other Government and industry organizations.

Several components are available in various degrees of maturity to achieve our goal of an intelligent mission. The most important aspect of an autonomous architecture is the ability to add, delete, and update the various components that combine to achieve an intelligent mission. The MDS is working to identify a file system and real-time database to be used on board the spacecraft. Another important architecture component is the middle ware that would encapsulate the hardware interface and other mission-unique components. We have written a publish/subscribe concept that can be used seamlessly between the flight and ground systems. This communication technology, developed by APL for the Navy, can be used in an embedded system and on commercially available workstations running various protocols spanning more than one machine connected by more than one interface. We ported this software to an APL flight testbed and demonstrated its feasibility. However, work is needed to make this communication technology more generic and flight worthy.

Generic Spacecraft Analysis Assistant (GenSAA) and GeNeric Inferential Executor (GENIE) are two tools that provide the ability to incorporate the domain knowledge expertise of instrument, systems, and subsystem engineers in the form of rules. These systems allow health and safety monitoring and day-to-day operations of a spacecraft to be automated. We used these tools not only to monitor the health and safety but also to recover from anomalies using the system and subsystem engineers’ knowledge. With the domain knowledge and expertise that we can capture, we can implement most, if not all, on-board fault detection and recovery schemes identified for the mission. Another intelligent ground system solution (ASPEN) is being explored in the area of planning and scheduling; it will help to schedule optimal science yield and optimize the use of the resources on board a spacecraft. JPL is working to move this software to flight readiness.

The Massachusetts Institute of Technology, JPL, Ames, and others are investigating two efforts in the area of instrument operation and control (Blue Fox) and an artificial intelligence (AI) engine. For example, Livingston (the second generation of Remote Agent) can capture the knowledge of the system, subsystem, and instrument engineers on board the spacecraft. Since this is the first line of defense for health and safety detection and resolution for a thinking spacecraft, these systems need to be of the highest quality and capability. APL will fund the follow-on work named MASC.

APL is working on two complementary efforts. The first is autonomous navigation (see page 66). APL is using the Global Positioning System for low-Earth orbit; for interplanetary navigation, APL did a research study using the Sun. This technology is ready to be inserted into a space mission. The other effort is man–machine interaction (see page 73), which addresses the problem of how to interface with an autonomous spacecraft.

All of the described systems are available but need more research into their effectiveness, ease of use, and capability. A missing link is the advanced concept of a spacecraft having the ability to adapt and learn.
**Rapid Application Development Environment for Analysis and Display of Spacecraft Data**  
*Amy K. Karlson and Martin R. Hall*

We proposed to develop a cross-platform environment to allow scientists to quickly and interactively build flexible analysis and display systems for spacecraft data. The system would be written in Java, allowing both the environment and resultant systems to be run on multiple platforms. The scientists would use the visual environment to select a representative data packet, choose filtering operations, and route the results to various display components. The result could be saved in the form of a cross-platform Java program that can take a real-time stream of packets, apply the filtering operations, and display the results. The data filters and display components would be represented as JavaBeans and would follow a standard application programming interface (API), permitting programmers to develop and incorporate new filters and display tools without modifying the development environment.

For this Advanced Technology Development (ATD) program, we have built a generic system that meets all of these objectives. In demonstrating the functionality of the environment, we implemented several reusable, customizable filter and display components for the Flexible Image Transport System (FITS) file format, the standard data interchange and archival format of the astronomy community. Because the environment allows scientists to select local or remote data sources, we thought an important extension to the proposed environment would be the capability to automatically discover data sources on the network. We therefore defined an API, much like those for filter and display components, to support plugging Java Jini services into the environment, which would automatically discover file or data services for a particular data type. We incorporated a FITS Jini service to demonstrate this capability. Finally, we briefed individuals at Goddard Space Flight Center on our system and plan to pursue potential follow-on work and a collaborative relationship with those individuals.

**Human Interface to Autonomous Operations**  
*Amy K. Karlson and John Gersh*

Advanced space mission concepts will involve increased levels of spacecraft autonomy to accomplish their objectives. Spacecraft will navigate, communicate, detect faults, reconfigure systems, and plan activities to achieve mission goals on their own. Instead of the current exchange of detailed command sequences and telemetry streams, any dialog between such a spacecraft and its users will center on higher-level mission goals, spacecraft states, and operational constraints; the dialog will involve current snapshots, history, and predictions for all of these things.

Under APL’s NASA ATD program, we have investigated the effects of this shift in the nature of the user–spacecraft dialog on user decision-making tasks, user-interface design, and overall ground-flight system software architecture.

Results from recent developments in user interaction with complex automation have been extended into this domain. This effort has indicated the need for explicit representation throughout the ground and flight system of *user expectations* of spacecraft states and plans. Departures from such expectations can also form the structure of the initial communication from a long-silent spacecraft and its depiction to users. The authority that has been delegated to the spacecraft for autonomous action in specific contexts also needs to be represented within the system and depicted to and controlled by users in a comprehensible, contextual way. Prototype display concepts and software architectural constructs have been investigated and related to general automated system requirements and to related spacecraft autonomy efforts, particularly those demonstrated on NASA’s Deep Space 1 mission.

This work can be generalized to other domains within which users interact with an autonomous planning agent, especially ones in which communication may be intermittent and time-delayed and the agent’s authority for autonomous action depends on users’ general delegation and on the situational context.
A major challenge facing the commercial space sector, NASA, and the Department of Defense (DoD) is to improve efficiency, reduce cycle time, and lower the cost of the spacecraft design, development, and procurement process. Attempts to accomplish this have led to a much larger dependence on modeling and simulation (M&S) earlier in a program’s life cycle. M&S is used to describe and simulate spacecraft and their related programs, including subsystems, mission operations, planning, scheduling, and analysis of science and mission products. It provides a means for testing new designs and technologies and can save time and cost through early detection of problems and anomalies. However, poor standards of interoperability and the lack of a general knowledge sustainment mechanism limit the increases in productivity that M&S could ultimately provide. In addition, the stand-alone nature of most M&S efforts hinders the amount of collaboration, innovation, and feedback among various groups of spacecraft engineers and scientists. Thus, currently, at its most basic level the design, development, and procurement process is not as efficient as it could be.

Our vision is to change this process radically, to replace it with a unified and standardized methodology in which M&S is combined with integration and testing in a seamless fashion so that the entire process is simplified and accelerated. Thus, in the initial stages, instead of a bevy of distinct special-purpose simulations and models, the designers will work with a virtual spacecraft—a fully integrated software representation of the product to be built, one that emulates its behavior. While each subsystem can be developed and tested individually, eventually all of these simulations can be brought together to provide a complete representation of the spacecraft. This virtual spacecraft will be realized through a distributed simulation that allows physically separated designers to collaborate. The virtual spacecraft will consist of a number of software objects that may exist at various levels of fidelity at any given time. As the project progresses, the fidelity of the various objects will increase. The fidelity will remain adjustable. Thus, the designer of the attitude system may require a very-high-fidelity simulation of a star camera but may tolerate (for reasons of computational efficiency) a very crude model of a battery. Indeed, in the initial stages of conceptual design, off-the-shelf models of some subsystems may be incorporated to start the process. However, as the design progresses, and fidelity increases, the virtual spacecraft nears its goal of full functionality.

We intend to provide a framework in which organizations can create models and simulations of individual spacecraft subsystem components that can interact in real time with other simulations, which may be distributed across the Internet. For example, let us suppose that the Acme Company markets a reaction wheel. A spacecraft engineer wishes to understand how this component will perform in a particular attitude control subsystem. Acme has a Web site that contains a catalog of the products they sell. From this Web site, the designer can download a simulation of a reaction wheel that has been...
written to conform to an industry-wide standard so that it can be integrated into the virtual spacecraft model in a plug-and-play fashion. Alternatively, the manufacturer can make available to the designer a simulation of its product that runs on a platform physically present at the company’s location. Over the Internet, the designer incorporates this object model simulation into a virtual spacecraft with confidence that it will function properly.

In addition to standardizing models to work over distributed heterogeneous platforms, we also envision a mechanism with which knowledge about spacecraft design and design processes can be sustained in the general spacecraft community. We define an approach that enables engineers to create “living” Web-based spacecraft descriptions that provide user-based views of current and historical spacecraft information and enable them to update information related to the spacecraft being viewed. This information and knowledge representation will help spacecraft designers and engineers make design choices based on the cumulative experience of the spacecraft design community.

Knowledge representation is at the core of our spacecraft design architecture. It is key to providing easy, flexible assembly and operation of distributed simulations in a collaborative, iterative, and rapid spacecraft design process. Knowledge representation insulates designers and system engineers from the details of assembling subsystem- and component-level simulations into a distributed simulation of an entire spacecraft. It also facilitates engineers’ ability to rapidly assemble distributed simulations to gain insight into the suitability of individual design choices and to store and retrieve such insights. Knowledge sustainment applies past design experience to help guide current and future designs.

In facilitating our framework, several tasks must be accomplished:
1. Industry-wide standards for distributed simulation and modeling of spacecraft must be defined.
2. A distributed simulation environment over wide area networks connecting heterogeneous platforms must be provided.
3. Tools to capture and retrieve design knowledge must be created.

These pieces must be tied together by a knowledge base that contains the standards, describes simulation components and their interfaces, captures designs, provides information that directs the execution of simulations on distributed computers, and provides living descriptions and experiences with spacecraft designs and design processes.

We have completed the following phases of work:
1. Standards Development—We have decomposed a generic spacecraft into functional subsystems and components and developed an initial list of component standards for attitude control components.
2. Simulation Environment—We have selected the DoD’s High-Level Architecture (HLA) as the test-bed distributed simulation environment architecture. We have developed a mechanism that automatically constructs HLA-compliant simulation components out of existing component simulation code and information about particular spacecraft designs.
3. Knowledge Sustainment—We have implemented a preliminary prototype system for selecting existing spacecraft designs that meet high-level mission criteria and for storing and retrieving virtual spacecraft simulation results with respect to quantitative performance requirements.
4. Knowledge Base—We have designed and implemented a knowledge base that includes representations of spacecraft component standards, components, designs, requirements, simulations, and design knowledge.

By the end of calendar year 2000, we plan to have demonstrated all these elements functioning together and simulating a simplified version of the Thermosphere-Ionosphere-Mesosphere Energetics and Dynamics (TIMED) spacecraft attitude-control system.
The goal of the Spacecraft Component Modeling Standardization effort is to facilitate the rapid development of mixed-fidelity distributed simulations of spacecraft through the combination of both new and legacy models in a plug-and-play fashion. Standardizing the interfaces of spacecraft component models enables the easy creation of a virtual spacecraft, which ties together all of the various subsystem components that typically are part of a satellite design. It enables system cost and performance trade-offs to be investigated early in the design process before any metal is cut or hardware is integrated.

The enabling technology for the rapid development of a virtual satellite is standardization of the interfaces of the various spacecraft component models. We used an object-oriented approach to formulate these standards. The standards are intended to be general enough to be usable in representing a wide variety of spacecraft; flexible enough to be easily modifiable to new circumstances, such as the use of newly developed components; and extensible in that they will define a set of core classes to which new classes and interactions can be added as needed.

Ultimately, any component simulation developed according to the standards will be assimilated into a larger, distributed simulation without its software or the software of other component simulations having to be changed. The component simulation software may model any behavior and perform any analysis that adequately represents the attributes of the component. Only the presentation of the data to be shared by a component model is standardized; no restrictions are placed on the modeling methods of the simulation developers. The details of each simulation are left entirely up to their developers. However, component models must support a minimum set of standard information to allow designers to compare and contrast them with other, similar components. Simulation components that are written using standards will be independent (and unaware) of other simulation components. Their standard interactions will facilitate incorporation into a virtual spacecraft and will be reusable in future mission simulations, thus amortizing the cost of modeling and simulation across missions.

We developed the standards by performing an object-oriented analysis of multiple spacecraft with different functions and purposes to extract their commonality. Spacecraft decomposition occurred along both functional and physical boundaries. Functionally, we identified and maintained the classical spacecraft subsystems: attitude determination and control, command and data handling, instruments/payload, mechanical and structural, navigation, power, propulsion, telecommunications, and thermal management. Physically, we captured properties such as the distribution of mass, the generation of heat, and data flow. We also defined standards for environmental models such as orbital propagators, gravitational models, magnetic field models, and atmospheric models so that the environment of the spacecraft could be adequately included in a distributed simulation.

Two types of information are required during the spacecraft design process to create a working model of a particular system: specification information and simulation information. Specification information is the design information that allows a spacecraft engineer to determine which components should be used in a particular design. Information of this type
includes attributes such as peak power, mass, and operational temperature range. Specification information can be used when a simulation is being compiled, but it is typically not passed dynamically at run time. Simulation information includes the attributes and interactions of a component that are computed and updated during a simulation. This type of information includes parameters such as instantaneous power use, momentum, and torque. This information, normally not used during the design phase, is important for simulating the effects that a component has on a larger system.

In addition to the attributes a component object inherits from the abstract classes, it also must possess a number of specific attributes unique to itself. For example, a reaction wheel object may inherit simulation information from the massive object and powered object classes, but it also possesses unique attributes such as wheel speed, wheel momentum, and wheel torque. The component is not required to include this information, but if it does, it is said to adhere to the standards of that class. In addition to these component-specific attributes, there may be a set of design-unique information. For example, the model for a fictitious Acme reaction wheel might include static and dynamic imbalance forces as part of its output in addition to those attributes required by its conformance to the standard (wheel speed and wheel momentum for this example).

Component and functional subsystem objects interact through method calls that set, access, or change attribute values. In addition, object attributes may be published to other objects. They form the overall representation of the spacecraft. However, they do not form a sufficient set for the simulation. They must be supplemented by an additional standard set that represents the environment of the spacecraft and the physics of its behavior. Thus, when the reaction wheel exerts a torque on the spacecraft, a spacecraft dynamics model calculates the change in the attitude that is, in turn, transmitted to the star tracker object to enable it to determine the positions of the stars it is sensing. These supplemental environmental and physical objects are also specified in the standards.

Following an object-oriented approach, we grouped the standardized information into various model classes. The standardized model objects include a set of abstract, inheritance classes. Various spacecraft components share physical characteristics. For example, they have mass; consume power; generate heat, electromagnetic noise, and perhaps jitter; and act as data sources or sinks. These physical characteristics are embodied in the attributes that the virtual spacecraft components inherit from a number of abstract classes. For example, a massive object class includes the attributes mass, center of mass, and moments of inertia, while the powered object class includes steady-state power, maximum power, heat generated, electromagnetic noise generated, and power status.
A layered information architecture is a key element in providing an environment for rapid and collaborative spacecraft design. It unifies object and interface standards, component simulations, spacecraft design, and knowledge sustainment while insulating designers from having to deal with the specifics of particular simulation environments or computing platforms.

Our information architecture involves a design process layer providing a designer’s view of a virtual spacecraft, expressed using standard design tools and product model formats; an abstract knowledge representation describing spacecraft object and modeling standards, components, and specific spacecraft and system designs; and a simulation layer that involves information necessary to distributed simulations in specific simulation environments.

The knowledge-representation layer, implemented as a knowledge base, is a significant result of our work. It also has a three-tiered architecture. The top, or standards tier, describes abstract classes, their standard methods and parameters, and inheritance hierarchy. This tier is populated with knowledge of standard physical classes (e.g., massive object and powered object) and methods for interacting with their instances (e.g., getMass() and getPower()). It is also populated with standards for component classes (e.g., reaction wheel and star tracker), their methods, and the standard classes from which they inherit.

The component tier describes specific spacecraft components and their simulations in terms of these standards. It is populated with specific component descriptions (e.g., Acme Reaction Wheel Model 6) and relates them to the abstract classes from which they inherit. Component descriptions and simulations may be hand-crafted by system designers or provided by component manufacturers and entered into the knowledge base. For example, a Reaction Wheel Model 6 simulation provided by Acme would be accompanied by a specification file and a simulation description file that can be entered into the knowledge base. The first provides specific values for standard reaction wheel parameters and specifies that the component object inherits its methods from the reaction wheel class. The second provides necessary information about the simulation code, as opposed to the actual reaction wheel.

The design tier represents system or spacecraft designs made up of particular selections and interconnections of these components. They’re made up of middle-tier component descriptions stored in the knowledge base and interconnected by spacecraft design tools that are capable of interacting with the knowledge base. This ATD project has developed a prototype tool that presents to a design engineer a palette of components. The designer can select the components of interest and connect them via their standard interfaces to create a design of a spacecraft subsystem or even a complete virtual spacecraft. The design is saved in an abstract representation to the lower tier of the knowledge base, which relates designs to components and captures component interconnections.

To establish a federated simulation of a particular design, we have developed software that automatically extracts design and component knowledge stored in the knowledge base and creates files that drive a simulation system. The formats of the generated files are determined by the needs of the simulation architecture. They describe to the simulation run-time the component simulation interfaces, interconnections, and locations of the simulation software. For our prototype, these files are in the formats needed by the DoD High Level Architecture infrastructure to instantiate simulation objects, specify their interrelationships, initialize their values, and run the distributed simulation.
Spacecraft design as it is currently practiced can be characterized as a multidisciplinary effort that involves a team of people who each make contributions to the final product. Design decisions are based on simulations and past designs, and the results of design iterations and key decisions must be made available for the next iteration. The rationale and context of design decisions are not generally captured. In summary, the design process is fragmented and hampered by communication gaps. The goal of the knowledge sustainment effort is to facilitate and improve the design process by bringing knowledge-based assistance to the task of making better and faster design decisions and capturing the decision-making basis and iterative system simulations required to arrive at a design.

The spacecraft design environment assumes a concept of operations in which a member of the spacecraft design team has focused on some component of the spacecraft or has an initial set of design requirements to satisfy. The choice of component plus some other menu selections sets the context for the knowledge-based assistance. In the process of making design decisions regarding the component, the knowledge sustainment element will allow the designer to review the results of past simulations and to retrieve relevant design knowledge as either design guidelines or similar design cases.

JHU/APL’s approach to knowledge sustainment makes context-sensitive design knowledge available to the designer through four capabilities: capture and retrieval of context-sensitive design requirements, capture and retrieval of design cases with similar context or requirements, capture and retrieval of context-sensitive design guidelines, and context-sensitive visualization of design performance. The current design sets the context for all knowledge-based assistance. The first thing a person might want to do is access the design requirements to establish the design goals. When a design is formulated and stored in the knowledge base, system and/or subsystem requirements are associated with the design components. Each stored requirement contains the parameters and associated values for which the requirement is specified. The designer can also access codified design knowledge or similar subsystem designs that have been accumulated from other design tasks. The user guides the process by selecting a focus for the design change, and the software retrieves all relevant knowledge (e.g., rules or cases) from the knowledge base. In the case of similar designs, a window of past designs and a measure of similarity (to the current design) are available to the designer for review, and the information associated with individual designs (e.g., requirements, annotation) is available through pop-up windows. This capability brings relevant past designs to the designer’s attention. The person synthesizes this information to make a design modification.

Once the design modification has been made, the person can elect to simulate the behavior of the revised design as discussed. After the simulation output is collected in a file, a process is executed that uses the knowledge about performance visualization to display the simulation results to the designer in the preferred format. On the basis of the results, the designer may choose to modify the design over multiple iterations to best meet the design requirements.

The final capability provided by the knowledge sustainment component is the ability to capture new design requirements and guidelines. The software provides a user-friendly set of tools that allows the designer to create and store new design requirements or guidelines at any point in the design process.
A spectrum of space-related technologies from APL